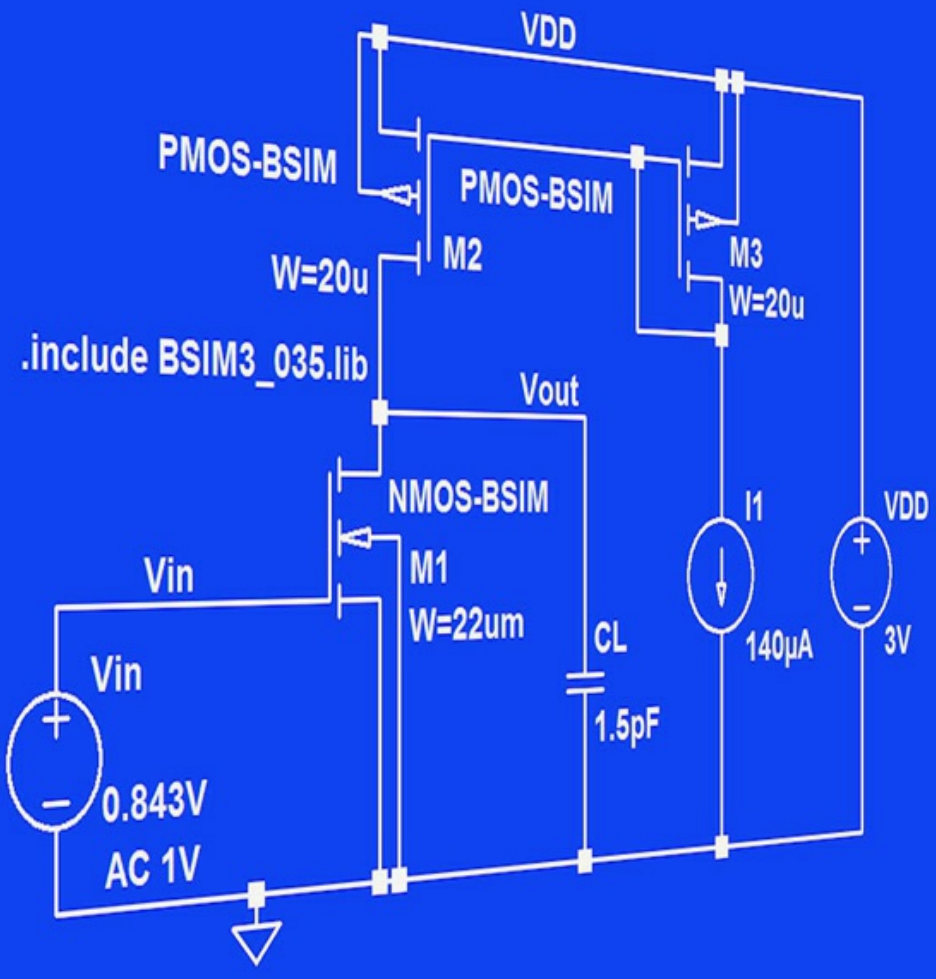
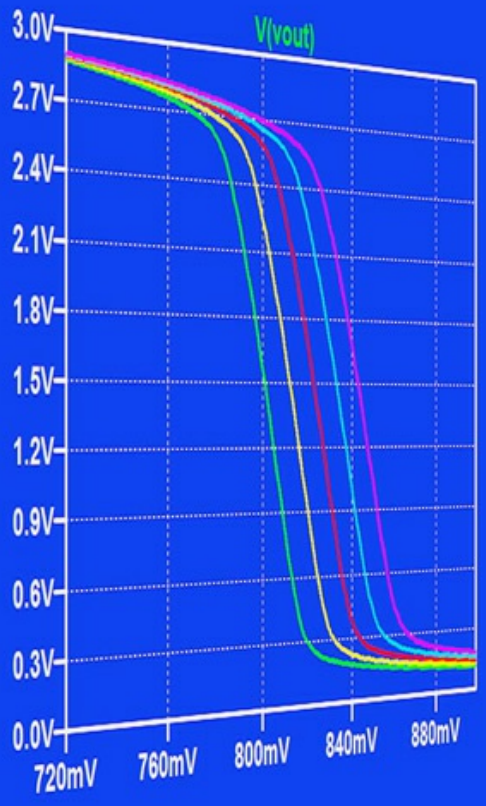
CMOS Integrated Circuit Simulation: Solutions

Erik Bruun





ERIK BRUUN

CMOS INTEGRATED CIRCUIT SIMULATION
SOLUTIONS

CMOS Integrated Circuit Simulation: Solutions
1st edition

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Preface

This book contains the end-of-chapter problems for each of the tutorials in the book 'CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide' (1st edition, 2015, also published by Bookboon) and provides solutions to the problems. For each of the problems, corresponding LTspice schematics are shown together with the simulation outputs resulting from running the simulation specified in the schematic. Also, the required interpretation of the simulation results is given.

Additionally, Appendix A contains a list of known (non-trivial) errors as of April 2016 in 'CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide' (1st edition, 2015).

Often, there is not just one possible way of solving the problems. Several options exist when drawing a schematic in LTspice and several different simulations may be specified in order to arrive at a solution, so the solutions given here should just be taken as examples of how the simulations may be performed.

The problems are reprinted from 'CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide', and page and figure references given in the problems are to pages and figures from this book. However, for convenience, several of the figures referred to in the problems are also shown here. When the problems refer to the BSIM transistor models from fig. 3.10 on page 77, fig. 6.2 on page 184 (or fig. P3.2 on page 98 and fig. P3.3 on page 99), you may turn to the Introduction in the present book to find out how to create the model file.

The simulations in this book have been performed using LTspice version 4.23j, dated 29 February 2016.

I hope you find the problems and solutions useful. If you find typos or errors, I would appreciate your feedback. Suggestions for improvement are also welcome. You may send them to me by email, eb@elektro.dtu.dk.

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Introduction

The file 'BSIM3_035.lib' is used in several of the problems in this book. It is derived from the file 'p35_model_card.inc' contained in the zip archive 'p35.zip' which can be downloaded from (Chan Carusone, Johns & Martin 2014). A few of the parameters in 'p35_model_card.inc' are deleted since they are ignored by LTspice anyway, and the parameters VTHO, TOX, UO, CJ, CJSW in 'p35_model_card.inc' which depend on process corners are given their nominal values for a typical process. The parameters which are deleted will not influence the simulation results significantly for normal values of transistor geometries. Also, the transistor models are named 'NMOS-BSIM' and 'PMOS-BSIM' rather than just 'NMOS' and 'PMOS' in order to emphasize that they are BSIM models, not just the default Spice models.

The following page shows the file 'p35_model_card.inc' with the modifications introduced for the model file 'BSIM3_035.lib' used in this book.

```
*p35 model cardBSIM 035.lib
.MODEL NMOS-BSIM NMOS                          LEVEL   =   49
+VERSION    =   3.1 TNOM    =   27  TOX =   '7.8E-9/proc_delta'
+XJ =   1E-07   NCH =   2.18E+17    VTH0    =   '0.48+vt_shift'
+K1 =   6.07E-01    K2  =   1.24E-03    K3  =   9.68E+01
+K3B    =   -9.84E+00   W0  =   2.02E-05    NLX =   1.62E-07
+DVT0W  =   0   DVT1W   =   0   DVT2W   =   0
+DVT0   =   2.87E+00    DVT1    =   5.86E-01    DVT2    =   -1.26E-01
+U0 =   '360*proc_delta*proc_delta' UA  =   -8.48E-10   UB  =   2.27E-18
+UC =   3.27E-11    VSAT    =   1.87E+05    A0  =   1.22E+00
+AGS    =   2.06E-01    B0  =   9.60E-07    B1  =   4.95E-06
+KETA   =   -1.67E-04   A1  =   0   A2  =   3.49E-01
+RDSW   =   8.18E+02    PRWG    =   2.35E-02    PRWB    =   -8.12E-02
+WR =   9.98E-01    WINT    =   1.55E-07    LINT    =   4.51E-10
+XL =   -5.00E-08   XW  =   1.50E-07   DWG =   -4.27E-09
+DWB    =   4.07E-09    VOFF    =   -4.14E-02   NFACTOR =   1.61E+00
+CIT    =   0   CDSC    =   2.39E-04    CDSCD   =   0.00E+00
+CDSCB  =   0   ETA0    =   1   ETAB    =   -1.99E-01
+DSUB   =   1   PCLM    =   1.32E+00    PDIBLC1 =   2.42E-04
+PDIBLC2    =   8.27E-03    PDIBLCB =   -9.99E-04   DROUT   =   9.72E-04
+PSCBE1 =   7.24E+08    PSCBE2  =   9.96E-04    PVAG    =   1.00E-02
+DELTA  =   1.01E-02    RSH =   3.33E+00    MOBMOD  =   1
+PRT    =   0   UTE =   -1.5    KT1 =   -1.11E-01
+KT1L   =   0   KT2 =   2.22E-02    UA1 =   4.34E-09
+UB1    =   -7.56E-18   UC1 =   -5.62E-11   AT  =   3.31E+04
+WL =   0   WLN =   9.95E-01    WW  =   0
+WWN    =   1.00E+00    WWL =   0   LL  =   0
+LLN    =   1   LW  =   0   LWN =   1
+LWL    =   0   CAPMOD  =   2   XPART   =   0.5
+CGDO   =   2.76E-10    CGSO    =   2.76E-10    CGBO    =   1.00E-12
+CJ =   '9e-4/proc_delta'   PB  =   7.95E-01    MJ  =   3.53E-01
+CJSW   =   '2.8e-10/proc_delta'    PBSW    =   7.98E-01    MJSW    =   1.73E-01
+CJSWG  =   1.81E-10    PBSWG   =   7.96E-01    MJSWG   =   1.74E-01
+CF =   0   PVTH0   =   -1.80E-02   PRDSW   =   -7.56E+01
+PK2    =   4.48E-05    WKETA   =   -1.33E-03   LKETA   =   -8.91E-03

.MODEL PMOS-BSIM PMOS                          LEVEL   =   49
+VERSION    =   3.1 TNOM    =   2.69E+01    TOX =   '7.8E-9/proc_delta'
+XJ =   1.00E-07    NCH =   8.44E+16    VTH0    =   '-0.6+vt_shift'
+K1 =   4.82E-01    K2  =   -2.13E-02   K3  =   8.27E+01
+K3B    =   -5  W0  =   5.24E-06    NLX =   2.49E-07
+DVT0W  =   0.00E+00    DVT1W   =   0   DVT2W   =   0
+DVT0   =   3.54E-01    DVT1    =   7.52E-01    DVT2    =   -2.98E-01
+U0 =   '150*proc_delta*proc_delta' UA  =   1E-10   UB  =   1.75E-18
+UC =   -2.27E-11   VSAT    =   2.01E+05    A0  =   1.04E+00
+AGS    =   2.90E-01    B0  =   1.94E-06    B1  =   5.01E-06
+KETA   =   -3.85E-03   A1  =   4.20E-03    A2  =   1.00E+00
+RDSW   =   4000    PRWG    =   -9.54E-02   PRWB    =   -1.92E-03
+WR =   1   WINT    =   1.47E-07    LINT    =   1.04E-10
+XL =   -4.98E-08   XW  =   1.51E-07   DWG =   -1.09E-08
+DWB    =   1.14E-08    VOFF    =   -1.29E-01   NFACTOR =   2.01E+00
+CIT    =   0   CDSC    =   2.40E-04    CDSCD   =   0
+CDSCB  =   0   ETA0    =   4.07E-02    ETAB    =   6.84E-03
+DSUB   =   3.21E-01    PCLM    =   5.96E+00    PDIBLC1 =   2.89E-03
+PDIBLC2    =   -1.45E-06   PDIBLCB =   -1E-03  DROUT   =   9.93E-04
+PSCBE1 =   7.88E+10    PSCBE2  =   5E-10   PVAG    =   15
+DELTA  =   9.96E-03    RSH =   2.6 MOBMOD  =   1
+PRT    =   0   UTE =   -1.5    KT1 =   -1.09E-01
+KT1L   =   0   KT2 =   2.19E-02    UA1 =   4.34E-09
+UB1    =   -7.62E-18   UC1 =   -5.63E-11   AT  =   3.28E+04
+WL =   0   WLN =   1   WW  =   0
+WWN    =   1.00E+00    WWL =   0   LL  =   0
+LLN    =   1   LW  =   0   LWN =   1
+LWL    =   0   CAPMOD  =   2.01E+00    XPART   =   0.5
+CGDO   =   2.10E-10    CGSO    =   2.12E-10    CGBO    =   1.00E-12
+CJ =   '14e-4/proc_delta'  PB  =   9.83E-01    MJ  =   5.79E-01
+CJSW   =   '3.2e-10/proc_delta'    PBSW    =   9.92E-01    MJSW    =   3.60E-01
+CJSWG  =   4.41E-11    PBSWG   =   9.85E-01    MJSWG   =   3.58E-01
+CF =   0   PVTH0   =   2.58E-02    PRDSW   =   -3.98E+01
+PK2    =   2.02E-03    WKETA   =   2.72E-03    LKETA   =   -7.14E-03
```

For several of the problems for tutorial 6, the file '`BSIM3_035PVT.lib`' is used. This file is derived from the file '`BSIM3_035.lib`' by introducing the speed parameters '`SN`' and '`SP`' for the process dependent parameters `VTHO`, `TOX`, `UO`, `CJ`, `CJSW`. The nominal values for typical process parameters are replaced by the expressions given below.

NMOS transistors:

$$\begin{aligned} \texttt{VTHO} &= \{0.48 - \texttt{SN}/10\} \\ \texttt{TOX} &= \{7.8\texttt{E} - 9/(1 + \texttt{SN}/20)\} \\ \texttt{UO} &= \{360 * (1 + \texttt{SN}/20) * *2\} \\ \texttt{CJ} &= \{9\texttt{e} - 4/(1 + \texttt{SN}/20)\} \\ \texttt{CJSW} &= \{2.8\texttt{e} - 10/(1 + \texttt{SN}/20)\} \end{aligned}$$

PMOS transistors:

$$\begin{aligned} \texttt{VTHO} &= \{-0.6 + \texttt{SP}/10\} \\ \texttt{TOX} &= \{7.8\texttt{E} - 9/(1 + \texttt{SP}/20)\} \\ \texttt{UO} &= \{150 * (1 + \texttt{SP}/20) * *2\} \\ \texttt{CJ} &= \{14\texttt{e} - 4/(1 + \texttt{SP}/20)\} \\ \texttt{CJSW} &= \{3.2\texttt{e} - 10/(1 + \texttt{SP}/20)\} \end{aligned}$$

References

Chan Carusone, T., Johns, D. & Martin, K. 2014, *Analog Integrated Circuit Design, Netlist and model files*. Retrieved from http://analogicdesign.com/students/netlists-models/

Tutorial 1 – Resistive Circuits

1.1

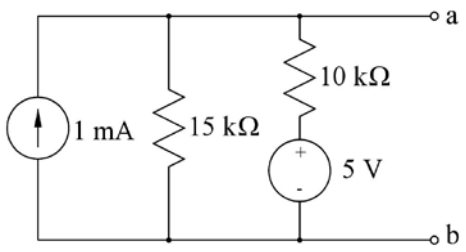
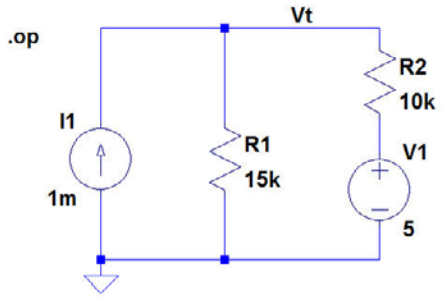


Figure P1.1

For the circuit shown in fig. P1.1, find the Thévenin voltage V_t and the Thévenin resistance R_t. A load resistor of $R_L = 3$ kΩ is now connected between the terminals a and b. Find the power dissipated in R_L.

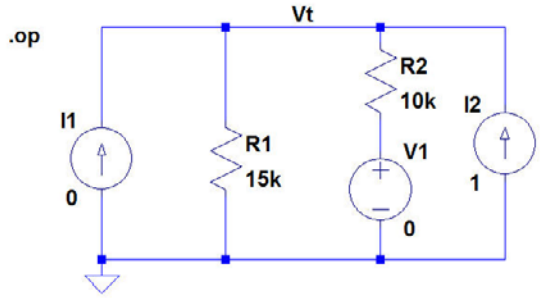
Solution:

For finding the Thévenin voltage V_t, we run the '.op' simulation shown below.
From the simulation output, we find $V_t = \mathtt{V(vt)} = 9$ V.



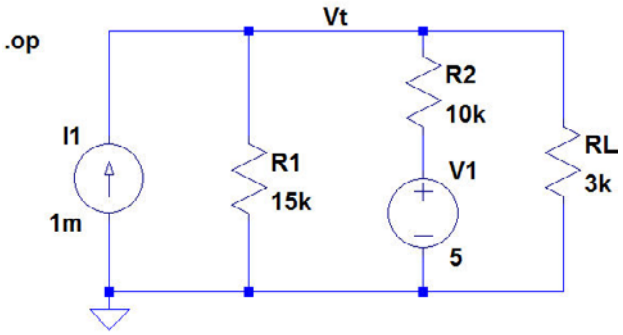

```
        --- Operating Point ---

V(vt):          9               voltage
V(n001):        5               voltage
I(I1):          0.001           device_current
I(R2):          0.0004          device_current
I(R1):          0.0006          device_current
I(V1):          0.0004          device_current
```

For finding the Thévenin resistance R_t, we reset the voltage source and the current source and apply a current source of 1 A between terminal a and b and find the voltage between a and b as shown below.
From the simulation output, we find $R_t = \mathtt{V(vt)}/1\text{ A} = 6$ kΩ.




```
        --- Operating Point ---

V(vt):          6000            voltage
V(n001):        0               voltage
I(I2):          1               device_current
I(I1):          0               device_current
I(R2):          0.6             device_current
I(R1):          0.4             device_current
I(V1):          0.6             device_current
```

For finding the power dissipated in a load resistor of $R_L = 3$ kΩ connected between the terminals a and b, we run the '.op' simulation shown below.
From the simulation output, we find P = `V(vt)I(Rl)` = 3 V × 0.001 A = 3 mW. By moving the cursor over `RL` after the simulation, the dissipation can also be read directly in the status bar at the bottom of the LTspice program window.




```
        --- Operating Point ---

V(vt):          3               voltage
V(n001):        5               voltage
I(I1):          0.001           device_current
I(Rl):          0.001           device_current
I(R2):          -0.0002         device_current
I(R1):          0.0002          device_current
I(V1):          -0.0002         device_current
```

1.2

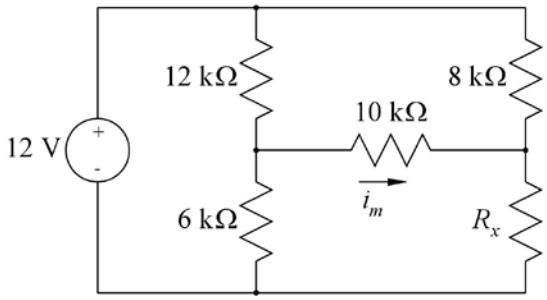
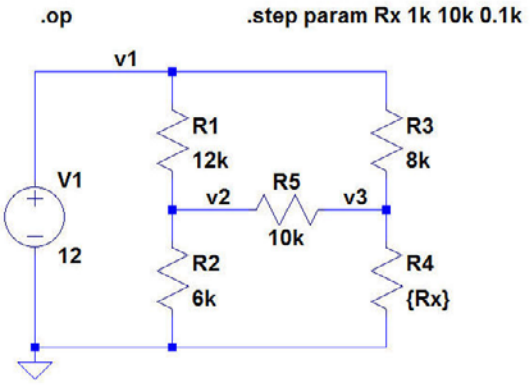


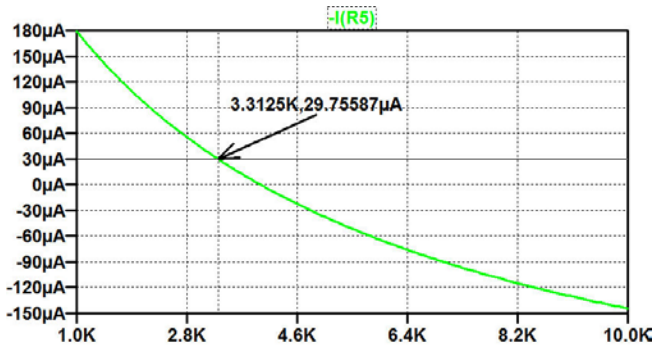
Figure P1.2

For the circuit shown in fig. P1.2, determine the value of resistor R_x so that the current i_m in the 10 kΩ resistor is 30 μA.

Solution:

For this circuit, we run a simulation where R_x is varied over a suitable range, and we plot i_m versus R_x. In the schematic below, $i_m =$ `-I(R5)` because `R5` is inserted with just one rotation of the resistor symbol, causing the positive direction of current flow in `R5` to be from right to left. From the simulation plot, we find that $R_x = 3.31$ kΩ results in $i_m = 30$ μA.





1.3

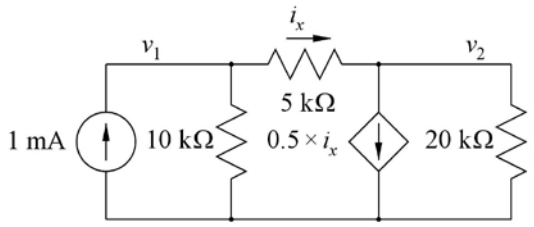
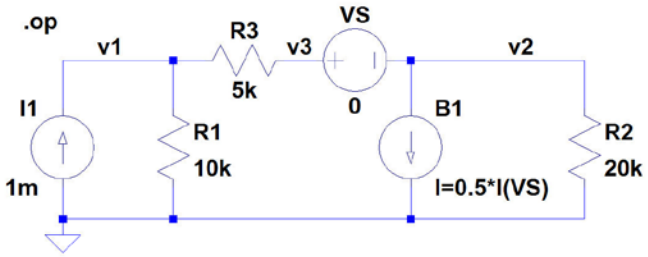


Figure P1.3

For the circuit shown in fig. P1.3, determine the value of the voltages v_1 and v_2 and the current i_x.

Solution:

For this circuit, we need a current controlled current source. This can be achieved using the arbitrary controlled current source as shown below. The voltage source `VS` is inserted because the controlling current must be the current through a voltage source. The current i_x is the current through `VS`.
From the output file, we find $v_1 = 6$ V, $v_2 = 4$ V and $i_x = \texttt{I(Vs)} = 0.4$ mA.




```
        --- Operating Point ---

V(v1):          6               voltage
V(v2):          4               voltage
V(v3):          4               voltage
I(B1):          0.0002          device_current
I(I1):          0.001           device_current
I(R3):          0.0004          device_current
I(R2):          0.0002          device_current
I(R1):          0.0006          device_current
I(Vs):          0.0004          device_current
```

1.4

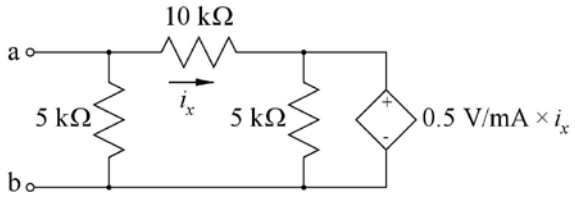
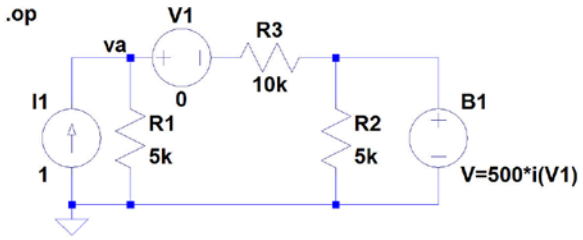


Figure P1.4

For the circuit shown in fig. P1.4, find the equivalent resistance looking into terminals a – b.

Solution:

For this circuit, we need a current controlled voltage source. This can be achieved using the arbitrary controlled voltage source as shown below. The voltage source `V1` is inserted because the controlling current must be the current through a voltage source. Additionally, a current source of 1 A is connected between terminals a and b, and the equivalent resistance is found as the voltage between a and b divided by 1 A. From the output file, we find R_{ab} = `V(va)`/1 A = 3.387 kΩ.




```
        --- Operating Point ---

V(va):          3387.1          voltage
V(n002):        161.29          voltage
V(n001):        3387.1          voltage
I(B1):          0.290323        device_current
I(I1):          1               device_current
I(R3):          0.322581        device_current
I(R2):          0.0322581       device_current
I(R1):          0.677419        device_current
I(V1):          0.322581        device_current
```

1.5

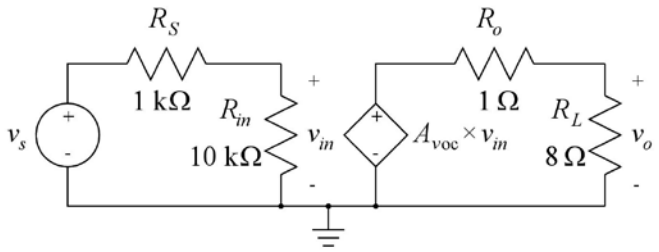
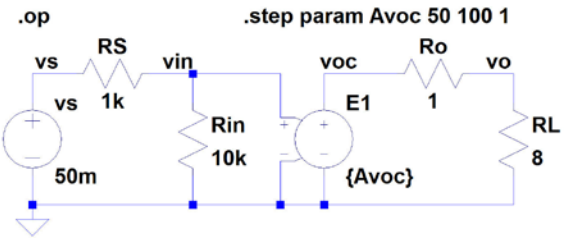


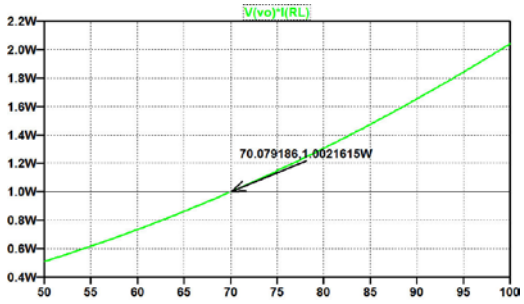
Figure P1.5

For the circuit shown in fig. P1.5, find the value of the gain A_{voc} which gives an output power in R_L of 1 W when the signal voltage v_s is 50 mV. With this value of A_{voc}, plot the output power versus the input voltage for v_s in the range from 0 mV to 100 mV.

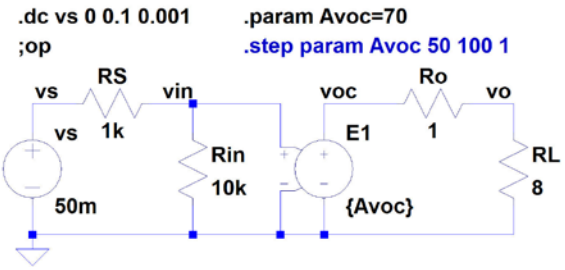
Solution:

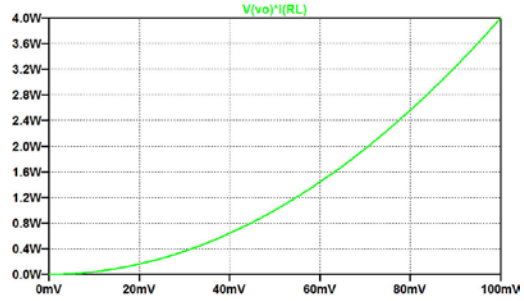
For this circuit, we define A_{voc} as a parameter and step it over a suitable range when running a '.op' simulation. From a plot of `V(vo)*I(RL)`, we find that $A_{voc} = 70$ V/V results in a power of 1 W in R_L, see simulation below.



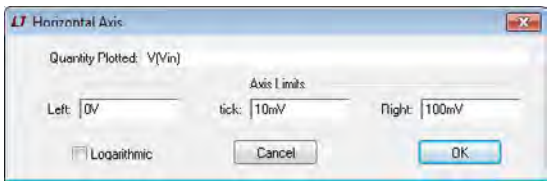


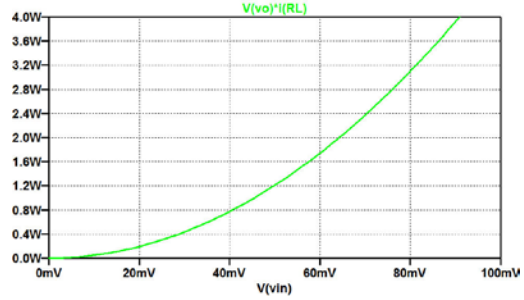
For simulating the output power versus the input voltage, we run a '.dc' simulation with the parameter `Avoc` set to 70, see simulation below, showing the output power versus v_s.





For showing the output power versus v_{in}, we move the cursor in the plot window to the x-axis and apply a left click on the mouse. This opens a specification window for the x-axis as shown below where we can change the 'Quantity Plotted' from `Vs` to `V(vin)`, resulting in a plot of the output power versus v_{in}.





1.6

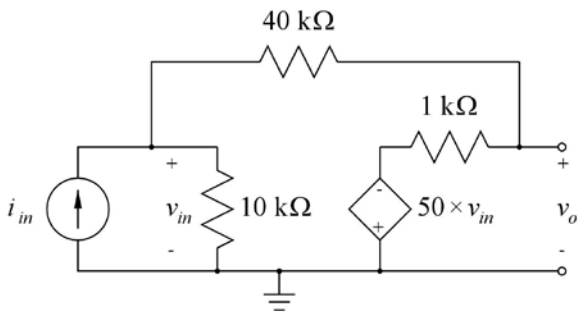
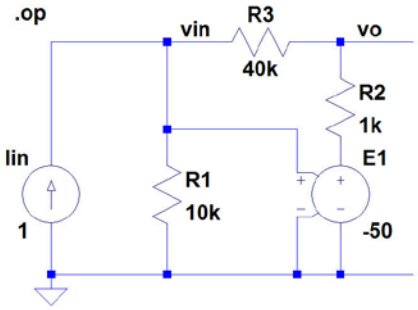


Figure P1.6

The circuit shown in fig. P1.6 is a transresistance amplifier built from an inverting voltage amplifier with an input resistance of 10 kΩ, an output resistance of 1 kΩ and an open circuit voltage gain of −50 V/V and a feedback resistor with a value of 40 kΩ. Find the open circuit transresistance R_{moc}, the input resistance R_{in} and the output resistance R_o of the resulting transresistance amplifier.

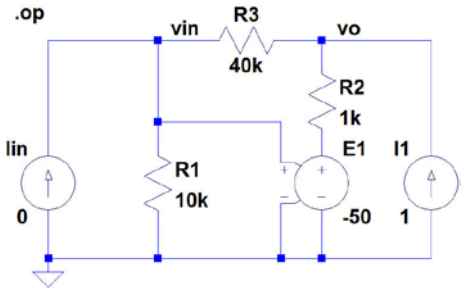
Solution:

For finding the open circuit transresistance R_{moc} and the input resistance R_{in}, we run a '.op' simulation with an input current signal source of 1 A, see below. The input resistance is found as v_{in}/i_{in} = V(vin)/1 A, and the transresistance is found as v_o/i_{in} = V(vo)/1 A.
From the output file, we find R_{moc} = V(vo)/1 A = -36.28 kΩ and R_{in} = V(vin)/1 A = 744 Ω.



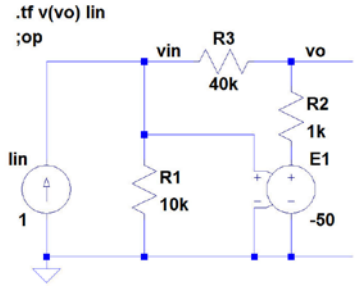

```
        --- Operating Point ---

V(vin):         744.102         voltage
V(vo):          -36279.5        voltage
V(n001):        -37205.1        voltage
I(Iin):         1               device_current
I(R2):          0.92559         device_current
I(R3):          -0.92559        device_current
I(R1):          0.0744102       device_current
I(E1):          0.92559         device_current
```

For finding the output resistance R_o, we run a '.op' simulation with a current source of 1 A connected to the output and with the input current source reset. The output resistance is found as `V(vo)`/1 A.
From the output file, we find R_o = `V(vo)`/1 A = 90.7 Ω.




```
--- Operating Point ---

V(vin):         18.1488         voltage
V(vo):          90.7441         voltage
V(n001):        -907.441        voltage
I(I1):          1               device_current
I(Iin):         0               device_current
I(R2):          0.998185        device_current
I(R3):          0.00181488      device_current
I(R1):          0.00181488      device_current
I(E1):          0.998185        device_current
```

An alternative simulation giving both input resistance, output resistance and transresistance in just one simulation is the '.tf' simulation shown below.




```
--- Transfer Function ---

Transfer_function:              -36279.5        transfer
iin#Input_impedance:            744.102         impedance
output_impedance_at_V(vo):      90.7441         impedance
```

1.7

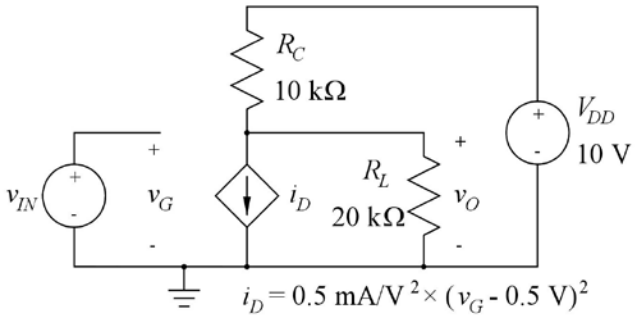
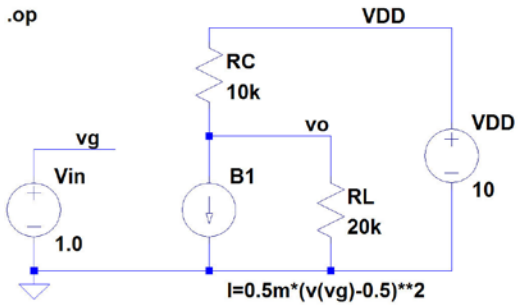


Figure P1.7

Fig. P1.7 shows a nonlinear transconductance amplifier. Find the values of bias voltages and currents for an input bias voltage (quiescent voltage) of $V_{IN} = 1.0$ V. Plot the output voltage v_O for the input voltage in the range from 0.5 V to 1.8 V. Find the small-signal voltage gain v_o/v_{in} for an input bias voltage of $V_{IN} = 1.0$ V and plot the small-signal voltage gain as a function of the input bias voltage for the input bias voltage in the range from 0.5 V to 1.8 V.

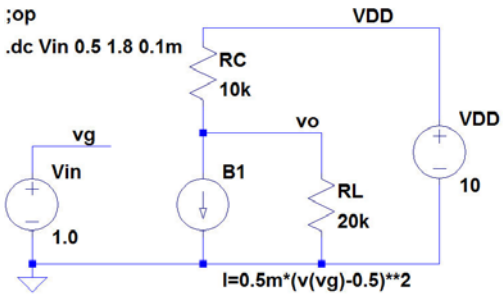
Solution:

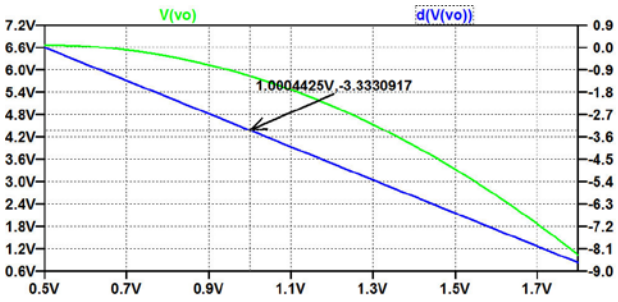
For finding the bias voltages and currents, we run a '.op' simulation as shown below.
From the output file, we find $I_D = \texttt{I(B1)} = 0.125$ mA, $I_C = \texttt{I(Rc)} = 0.417$ mA, $I_L = \texttt{I(Rl)} = 0.292$ mA and $V_O = \texttt{V(vo)} = 5.83$ V.



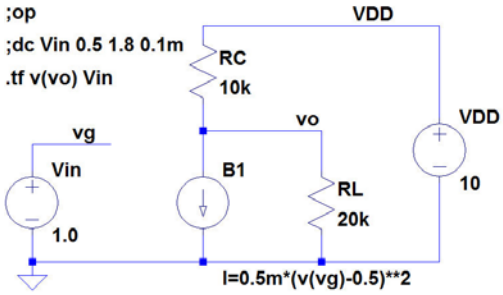

```
        --- Operating Point ---

V(vdd):         10              voltage
V(vo):          5.83333         voltage
V(vg):          1               voltage
I(B1):          0.000125        device_current
I(Rl):          0.000291667     device_current
I(Rc):          0.000416667     device_current
I(Vin):         0               device_current
I(Vdd):         -0.000416667    device_current
```

For plotting the output voltage and the small-signal voltage gain versus input bias voltage, we run a '.dc' simulation as shown below. The voltage gain is shown as the derivative of the output voltage, `d(V(vo))`.





The small-signal gain for $V_{IN} = 1.0$ V may be found from the plot above, or it may be found from a '.tf' simulation as shown below. From this, we find a small-signal gain of -3.33 V/V.




```
        --- Transfer Function ---

Transfer_function:            -3.33333        transfer
vin#Input_impedance:          1e+020          impedance
output_impedance_at_V(vo):    6666.67         impedance
```

1.8

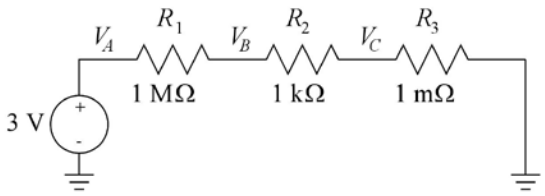
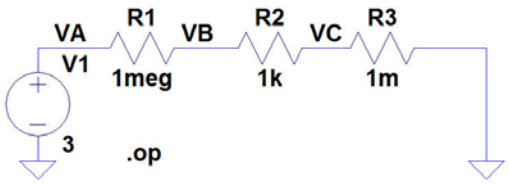


Figure P1.8

Fig. P1.8 shows a series connection of three resistors and a voltage source.
Try three different ways of drawing the schematic:
(1): Insert the components and draw the connections between them.
(2): Insert the components (including the ground symbols) and draw an unbroken wire (hotkey 'F3') from leftmost ground symbol across the components to rightmost ground symbol.
(3): Insert the ground symbols, draw an unbroken wire between them, and then insert the component directly on top of the wire.
Observe how LTspice 'cleans up' the wiring.
Find the voltages V_A, V_B and V_C.

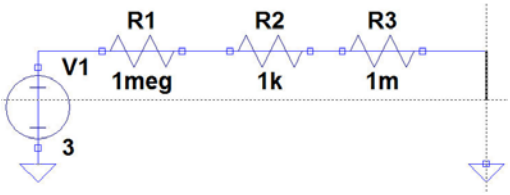
Solution:

(1) The figure below shows the resulting schematic and the output file for a '.op' simulation. From the output file, we find $V_A = 3.0000$ V, $V_B = 2.997$ mV and $V_C = 2.997$ nV.

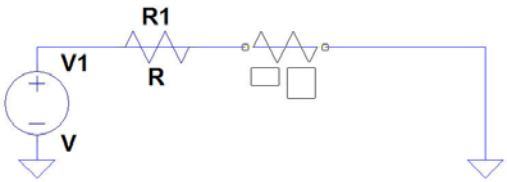



```
        --- Operating Point ---

V(vb):          0.00299701      voltage
V(va):          3               voltage
V(vc):          2.997e-009      voltage
I(R3):          -2.997e-006     device_current
I(R2):          -2.997e-006     device_current
I(R1):          -2.997e-006     device_current
I(V1):          -2.997e-006     device_current
```

(2) When inserting the components and drawing a wire across the components, the wire appears across the components during the insertion process as shown in the figure below, but when the insertion is completed, the wiring is cleaned up, resulting in the schematic shown above.



(3) When inserting an unbroken wire first and the components afterwards on top of the wire, the cleaning up takes place when completing the insertion. The figure below shows the schematic when the voltage source insertion has been completed and the resistor insertion is in progress.



Tutorial 2 – Circuits with Capacitors and Inductors

2.1

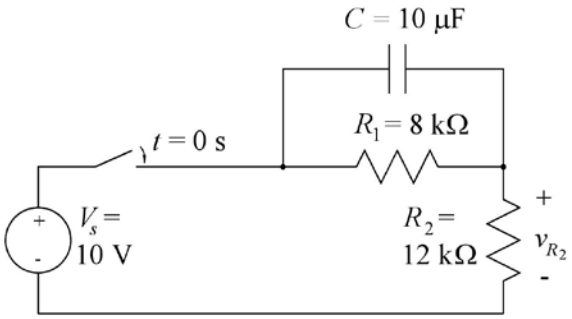
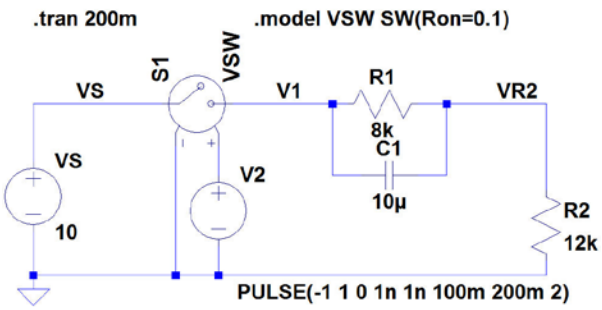


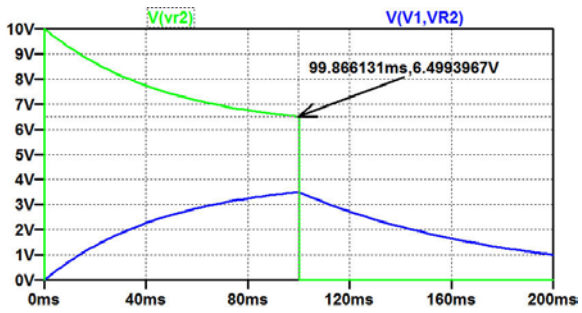
Figure P2.1

For the circuit shown in fig. P2.1, assume that the switch is closed at time $t = 0$ and re-opened at time $t = 100$ ms. Find the value of the voltage v_{R_2} immediately after the switch is closed. Find the value of v_{R_2} immediately before the switch is re-opened. Find the value of v_{R_2} immediately after the switch is re-opened. Plot v_{R_2} versus time for $0 \leq t \leq 200$ ms. Plot the capacitor voltage versus time and find the time constants for the charging and discharging of the capacitor C.

Solution:

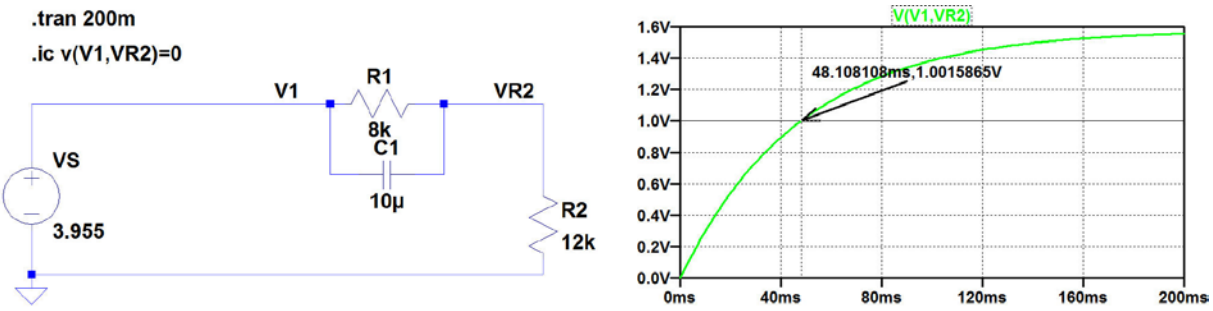
The figure below shows the circuit with a voltage controlled switch, controlled by a voltage V2 specified as a time varying voltage. For the specification, we use a 'PULSE' waveform with rise time and fall time of 1 ns which is much shorter than the pulse width of 100 ms. For the voltage controlled switch, a '.model' specification has been inserted, changing the on-resistance from the default value of 1 Ω to a value of 0.1 Ω. From the figure, we find the value of v_{R_2} immediately after the switch is closed to be 10 V, and we find the value of v_{R_2} immediately before the switch is re-opened to be 6.5 V. The value of v_{R_2} immediately after the switch is re-opened is found to be 0 V.



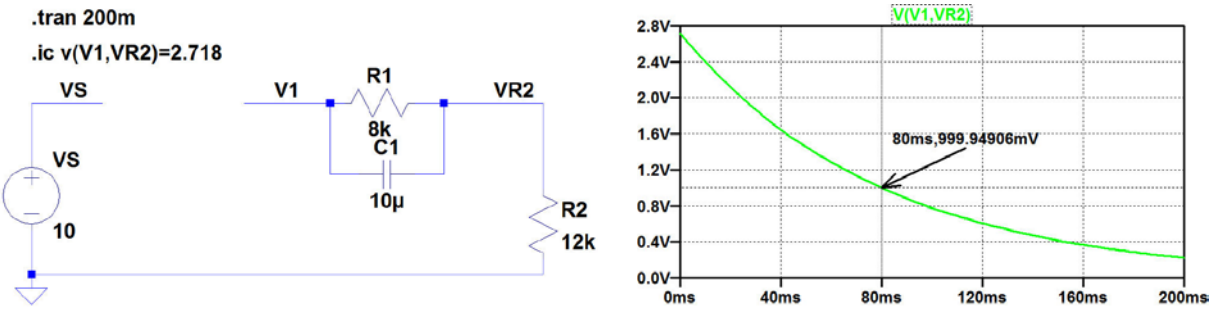


The time constants for charging and discharging of the capacitor may be evaluated from the previous simulation but an easier, alternative approach is to run transient simulations with only dc voltage sources and a specification of initial voltages for the capacitor.

The figure below shows a simulation for finding the charging time constant. As the limiting value of v_{R_2} for $t \to \infty$ is $V_S R_1/(R_1+R_2)$, it is convenient to select $V_S = (1+R_2/R_1)/(1-e^{-1}) = 3.955$ V, implying that a capacitor voltage of 1 V is reached for $t = \tau$. Also, the initial value of the capacitor voltage must be specified to 0 V. From the figure, we find $\tau = 48$ ms.



For finding the time constant for discharging with the switch open, we disconnect V_S and specify the initial value of the capacitor voltage to be e = 2.718 V so that the capacitor voltage reaches a value of 1 V after $t = \tau$, see figure below. From this simulation, we find $\tau = 80$ ms.



2.2

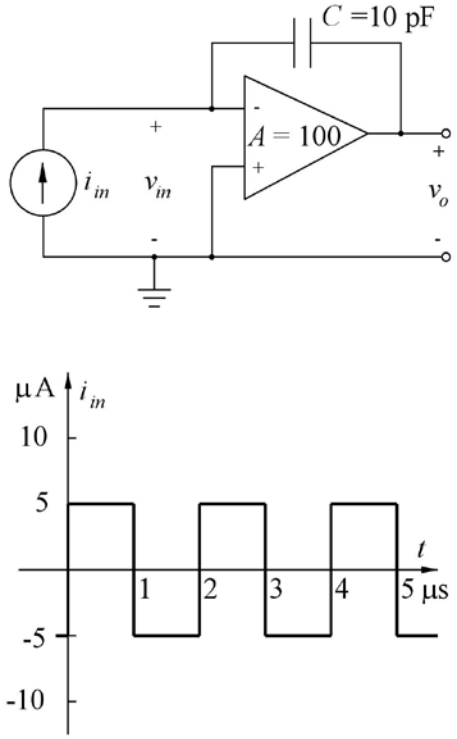
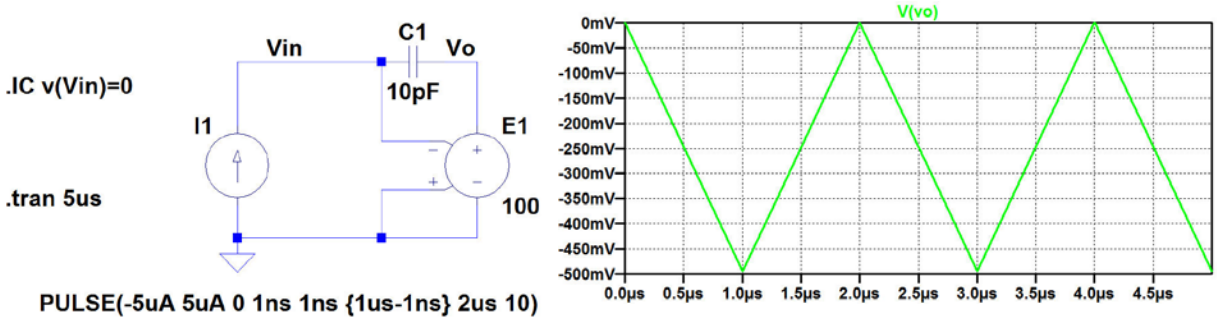


Figure P2.2

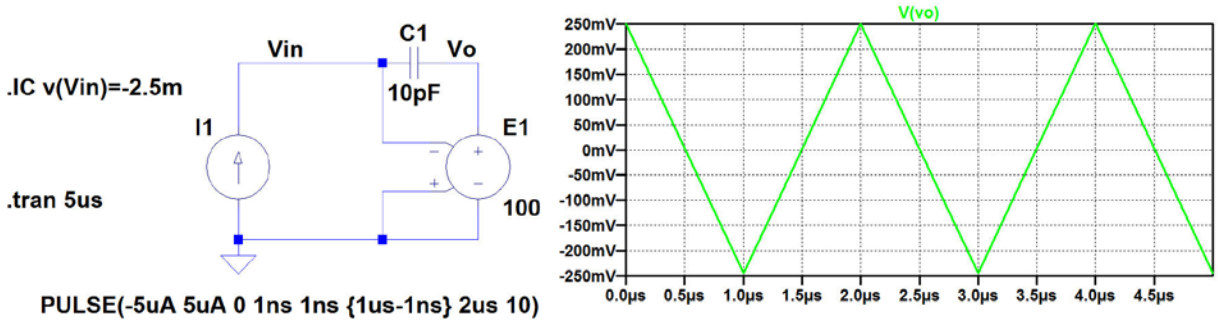
For the circuit shown in fig. P2.2, plot the output voltage v_o versus time t for $0 \leq t \leq 5$ μs. You may assume that the amplifier has infinite input resistance and zero output resistance. Also, assume that the initial value of the input and output voltage at $t = 0$ is 0 V. Which initial value of the input voltage v_{in} will result in a mean value of 0 V for the output voltage v_o?

Solution:

The figure below shows the circuit with the amplifier modelled by a voltage controlled voltage source. The time varying input current is specified by a '`PULSE`' waveform with rise time and fall time of 1 ns which is much shorter than the pulse width of 1 μs, and with the specification shown below, the mean input current is 0. The initial value of the input voltage is set by the '`.IC`' directive.



From the plot of the resulting output waveform, we find a mean value of -250 mV for the output voltage, so in order to obtain a mean value of 0 V for the output voltage, the initial value of the input voltage must be changed by -2.5 mV since the gain of the inverting voltage controlled voltage source is 100. Thus, the required initial value of v_{in} is -2.5 mV as confirmed by the simulation shown below.



2.3

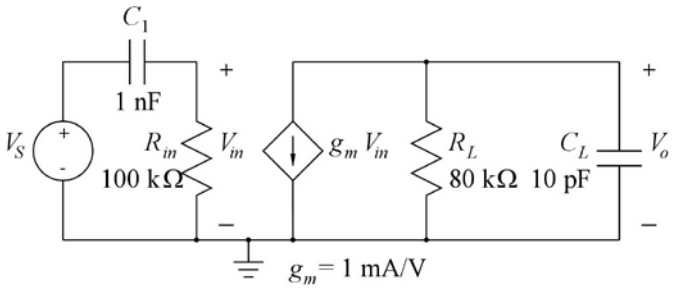
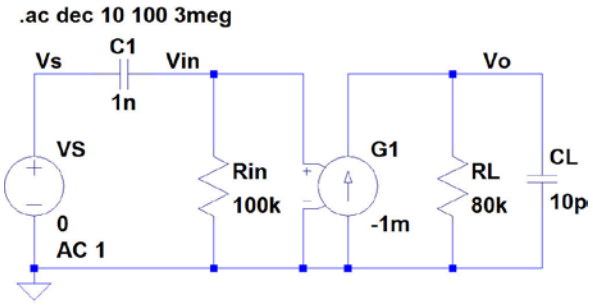


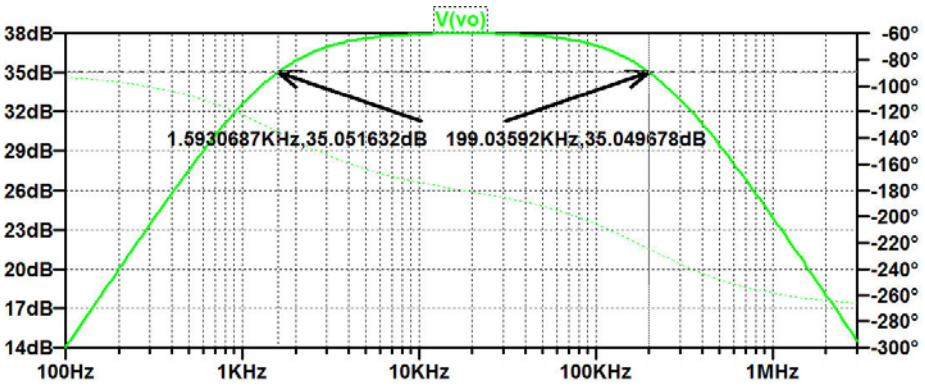
Figure P2.3

For the circuit shown in fig. P2.3, find the midband gain, the upper and lower half-power (−3 dB) frequencies and the 3-dB bandwidth. Plot the output voltage V_o versus frequency in a Bode plot covering a frequency range which extends from approximately one decade below the lower half-power frequency to approximately one decade above the upper half-power frequency.

Solution:

The figure below shows the circuit and the simulated Bode plot from 100 Hz to 3 MHz. From the Bode plot, we find a midband gain of 38 dB, a lower −3 dB frequency of 1.59 kHz and an upper −3 dB frequency of 199 kHz. The 3-dB bandwidth is 199 kHz − 1.59 kHz = 197.41 kHz.





2.4

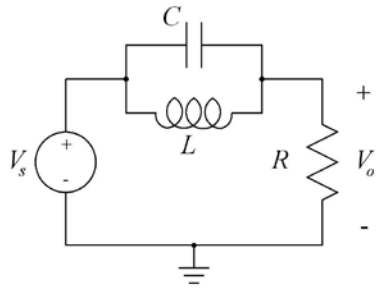
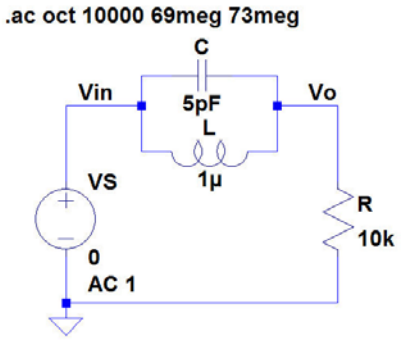


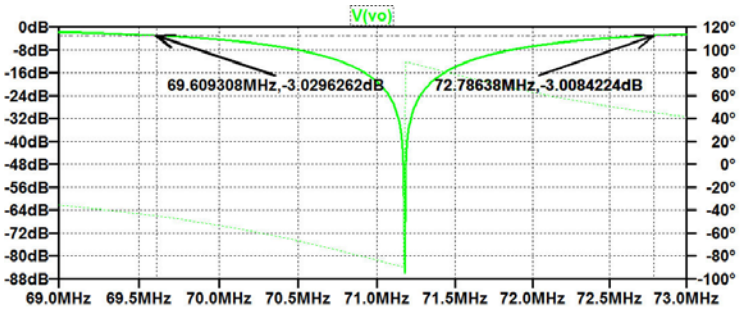
Figure P2.4

For the notch filter shown in fig. P2.4, plot V_o versus frequency in a frequency range showing the notch and the 3-dB bandwidth. Assume $L = 1$ μH, $C = 5$ pF and $R = 10$ kΩ. From the plot, find the notch frequency, the bandwidth and the quality factor Q.

Solution:

The figure below shows the circuit and the simulated Bode plot from 69 MHz Hz to 73 MHz. Notice that a large number of points per octave has been specified (10000) in order to show the notch. In order to find the frequency range to plot, it may be a good idea to calculate the resonance frequency from $f_{res} = (2\pi\sqrt{LC})^{-1} = 71.18$ MHz. From the Bode plot, we find a notch frequency of 71.2 MHz, a 3-dB bandwidth of $(72.79 - 69.61)$ MHz = 3.18 MHz and a quality factor $Q = 71.2/3.18 = 22.4$.
Analytically, the quality factor is calculated from $Q = R\sqrt{C/L} = 22.4$.





2.5

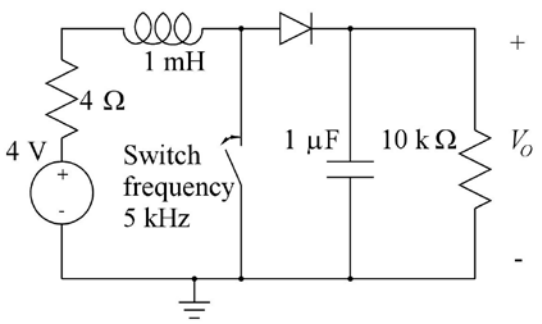
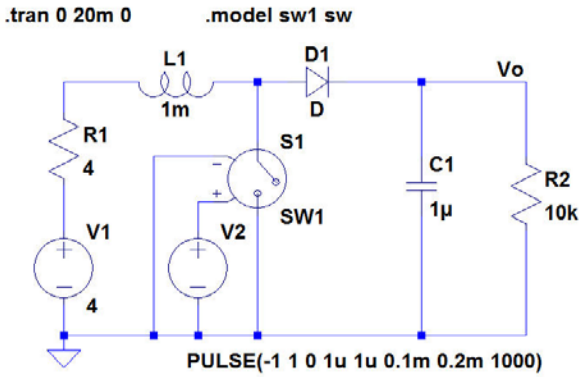


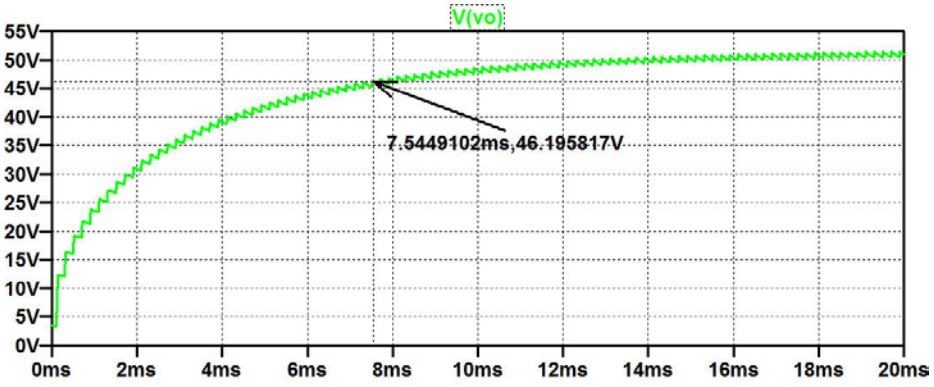
Figure P2.5

The circuit shown in fig. P2.5 is a dc-dc converter which converts a dc voltage of 4 V into a high voltage V_O. The switch is an electronic switch which opens and closes with a frequency of 5 kHz and a duty cycle of 50%, starting at time $t = 0$. The diode can be assumed to be modeled by the default Shockley diode model. Initially, the current in the inductor is 0 and the output voltage V_O is 0. Find the dc output voltage for $t \to \infty$ and find the time required for V_O to reach 90% of the final value.

Solution:

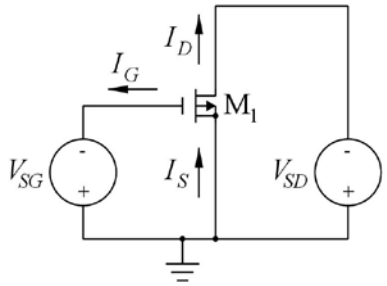
The figure below shows the circuit with a voltage controlled switch controlled by a voltage V2 specified as a time varying voltage. For the specification, a 'PULSE' waveform with rise time and fall time much shorter than the pulse width is used. For the diode, no '.model' specification is needed for the default Shockley model. For the voltage controlled switch, a '.model' specification has been inserted using the default switch parameters. If you do not insert the '.model' specification, the simulation will still run with the default switch model but an error message will be produced.
The figure below shows the simulated output voltage from 0 to 20 ms. From the simulation, we find an output voltage of about 51 V for $t \to \infty$ and a rise time of about 7.5 ms for reaching 90% of the final value.





Tutorial 3 – MOS Transistors

3.1



$W = 10$ µm, $L = 1$ µm

$K_p = 55$ µA/V^2, $V_{to} = -0.71$ V, $\lambda = 0.16$ V^{-1},

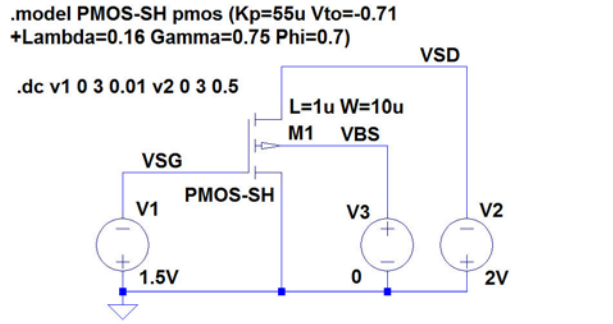
$\gamma = 0.75\ \sqrt{\text{V}}$, $|2\Phi_F| = 0.7$ V.

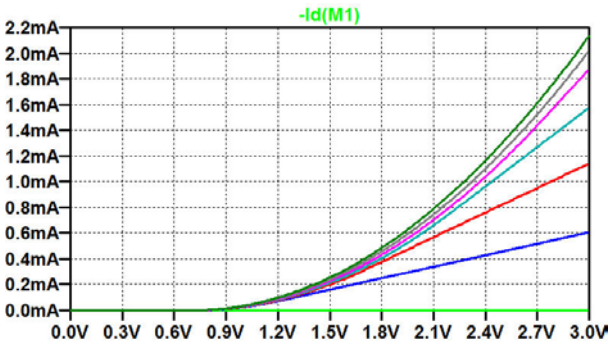
Figure P3.1

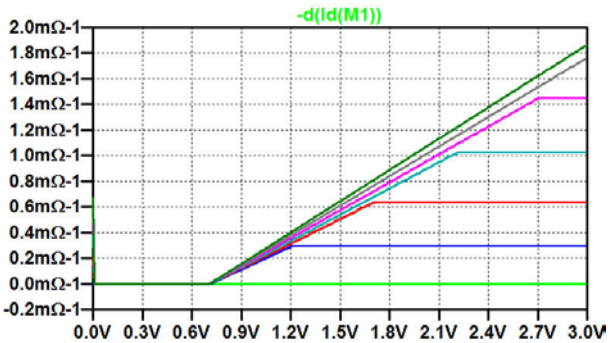
For the PMOS transistor shown in fig. P3.1, simulate and plot the input characteristics I_D versus V_{SG} and $\partial i_D/\partial v_{SG}$ for $V_{SD} = 0$, 0.5, 1.0, 1.5, 2.0, 2.5 and 3.0 V. Use the model parameters and transistor dimensions shown in the figure. Find the bias current I_D and the small-signal parameters g_m, g_{mb} and g_{ds} for a bias point of $V_{SG} = 1.5$ V and $V_{SD} = 2.0$V.

Solution:

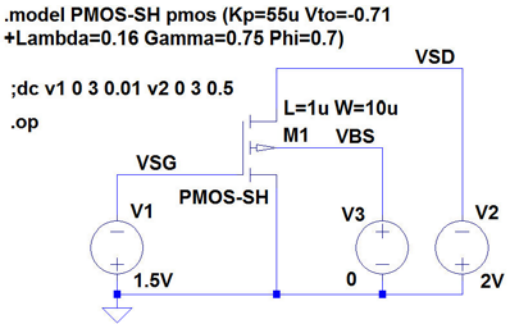
The figure below shows the schematic for simulating the input characteristics. Also shown are the resulting plots of I_D versus V_{SG} and $\partial i_D/\partial v_{SG}$ (or g_m) for $V_{SD} = 0$ V (green curves), 0.5 V (blue curves), 1.0 V (red curves), 1.5 V (cyan curves), 2.0 V (purple curves), 2.5 V (grey curves) and 3.0 V (dark green curves). You may notice that when the transistor is in the triode region ($|V_{DS}| < |V_{GS}| - |V_t|$), g_m is independent of V_{SG}, see equation (3.11) in 'CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide'.







For finding the bias current and the small-signal parameters for a bias point of $V_{SG} = 1.5$ V and $V_{SD} = 2.0$ V, we run a '.op' simulation. The bias values and the small-signal parameters are given in the error log file ('Ctrl-L') from this simulation, see below where the requested parameters are underlined. Notice that in LTspice, the drain current is defined positive into the transistor, whereas in fig. P3.1, it is defined positive out of the transistor.




```
Semiconductor Device Operating Points:
                        --- MOSFET Transistors ---
Name:                m1
Model:            pmos-sh
Id:            -2.27e-04
Vgs:           -1.50e+00
Vds:           -2.00e+00
Vbs:            0.00e+00
Vth:           -7.10e-01
Vdsat:         -7.90e-01
Gm:             5.74e-04
Gds:            2.75e-05
Gmb:            2.57e-04
```

3.2

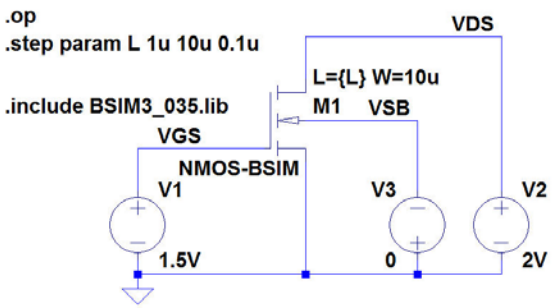
```
.MODEL NMOS-BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = 360 UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03
```

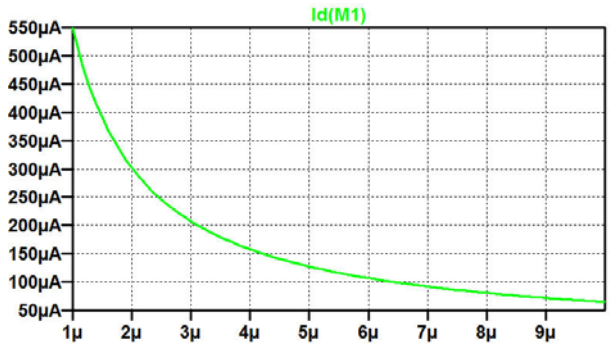
Figure P3.2

For an NMOS transistor with the transistor model shown in fig. P3.2 (BSIM3 0.35 µm model, fig. 3.10) and channel width $W = 10$ µm, simulate and plot I_D versus the channel length L in the interval 1 µm $< L <$ 10 µm for a bias point of $V_{GS} = 1.5$ V, $V_{DS} = 2.0$ V and $V_{SB} = 0$ V. Find the bias current I_D and the small-signal parameters g_m, g_{mb} and g_{ds} for $L = 1$ µm and for $L = 5$ µm in the bias point.
Hint: Define L as a parameter, compare page 26.

Solution:

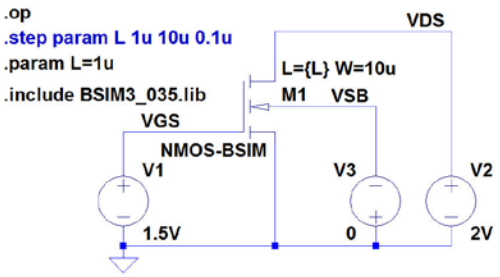
The figure below shows the schematic for simulating the drain current. The channel length L is defined as a parameter which is stepped from 1 µm to 10 µm. The transistor model is included in a separate model file, '`BSIM3_035.lib`'. The drain current is found from a '.op' simulation.





For finding the bias current I_D and the small-signal parameters g_m, g_{mb} and g_{ds} for $L = 1$ µm and for $L = 5$ µm in the bias point of $V_{GS} = 1.5$ V, $V_{DS} = 2.0$ V and $V_{SB} = 0$ V, we specify the value of L using a '.param' directive with the '.step param' directive changed into a comment, see the figure on the following page with $L = 1$ µm.

The bias point information is given in the error log file from a '.op' simulation. The error log files for $L = 1$ µm and $L = 5$ µm are shown below with an underlining of the requested parameters. We notice that with the BSIM transistor model, neither the bias current, nor the transconductances (g_m and g_{mb}) scale by a factor of 5 as predicted by the Shichman-Hodges model.



L=1e-6:

Semiconductor Device Operating Points:
--- BSIM3 MOSFETS ---

Name:	m1
Model:	nmos-bsim
Id:	5.48e-04
Vgs:	1.50e+00
Vds:	2.00e+00
Vbs:	0.00e+00
Vth:	5.43e-01
Vdsat:	6.21e-01
Gm:	9.92e-04
Gds:	1.03e-05
Gmb	2.63e-04

L=5e-6:

Semiconductor Device Operating Points:
--- BSIM3 MOSFETS ---

Name:	m1
Model:	nmos-bsim
Id:	1.27e-04
Vgs:	1.50e+00
Vds:	2.00e+00
Vbs:	0.00e+00
Vth:	5.10e-01
Vdsat:	7.45e-01
Gm:	2.45e-04
Gds:	1.94e-06
Gmb	6.53e-05

3.3

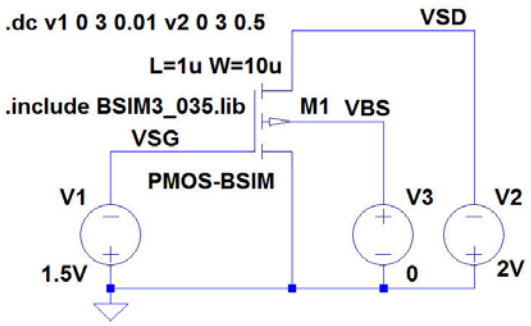
```
.MODEL PMOS-BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.8E-9
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = 150 UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

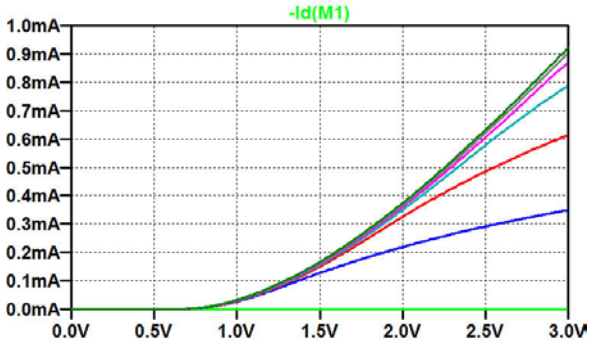
Figure P3.3

For a PMOS transistor with the transistor model shown in fig. P3.3 (BSIM3 0.35 µm model, fig. 3.10) and channel width $W = 10$ µm and channel length $L = 1$ µm, simulate and plot the input characteristics I_D versus V_{SG} for $V_{SD} =$ 0, 0.5, 1.0, 1.5, 2.0, 2.5 and 3.0 V. Assume $V_{BS} = 0$ V. Also simulate and plot the output characteristics I_D versus V_{SD} for $V_{SG} = 0$, 0.5, 1.0, 1.5, 2.0, 2.5 and 3.0 V. Use the cursors to find I_D and $\partial i_D/\partial v_{SD}$ for $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V.

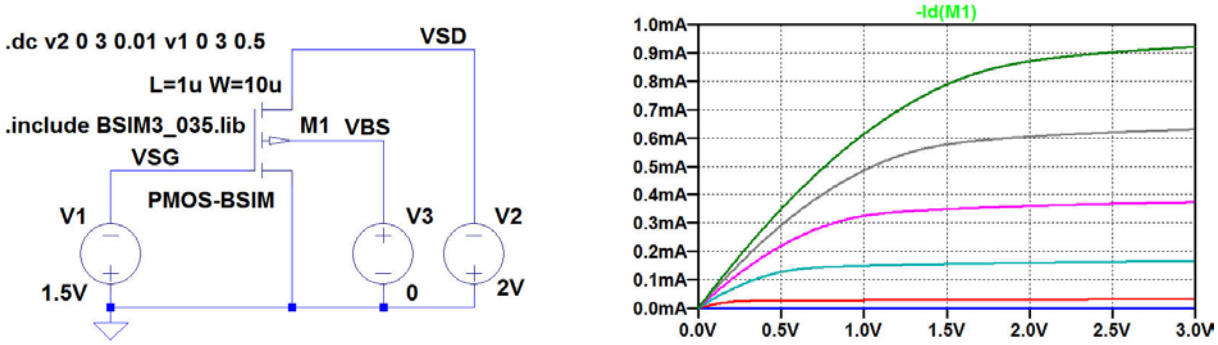
Solution:

The figure below shows the schematic for simulating the input characteristics. Also shown is the resulting plot of I_D versus V_{SG} for $V_{SD} = 0$ V (green curve), 0.5 V (blue curve), 1.0 V (red curve), 1.5 V (cyan curve), 2.0 V (purple curve), 2.5 V (grey curve) and 3.0 V (dark green curve). Because of the difference in sign conventions between textbooks and LTspice, the plot below shows `-Id(M1)` which is equal to I_D using the normal textbook convention.

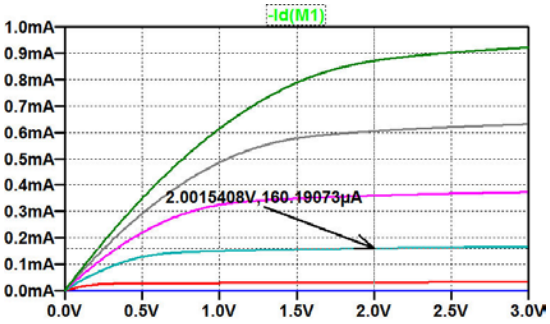




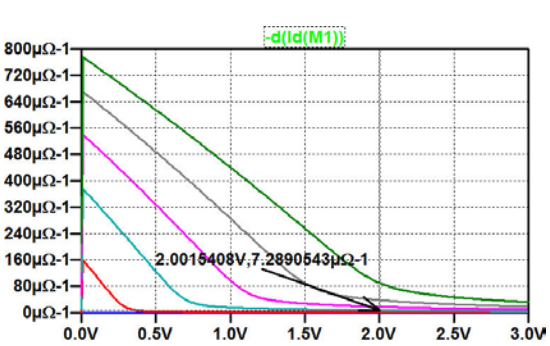
The figure below shows the schematic for simulating the output characteristics. Also shown is the resulting plot of I_D versus V_{SD} for $V_{SG} = 0$ V (green curve, not visible because of the blue curve), 0.5 V (blue curve), 1.0 V (red curve), 1.5 V (cyan curve), 2.0 V (purple curve), 2.5 V (grey curve) and 3.0 V (dark green curve).

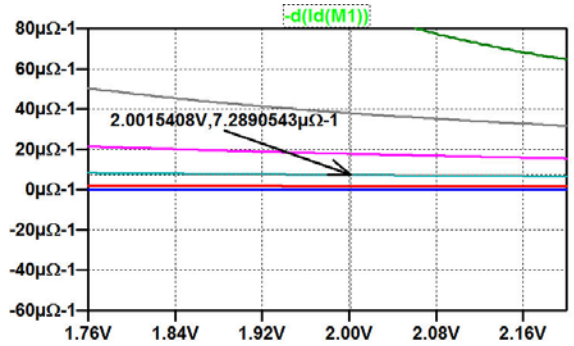


For finding I_D for $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V, the output characteristics above are used with a cursor placed on the cyan curve, see figure below. The cursor is shifted from one curve to another by the up/down arrow keys. We find $I_D = 0.16$ mA.



For finding $\partial i_D/\partial v_{SD}$ for $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V, the derivative of I_D is plotted as shown below. It may be a good idea to zoom in on the relevant part of the characteristics as also shown in the figure. We find $\partial i_D/\partial v_{SD} = 7.3$ µA/V.





3.4

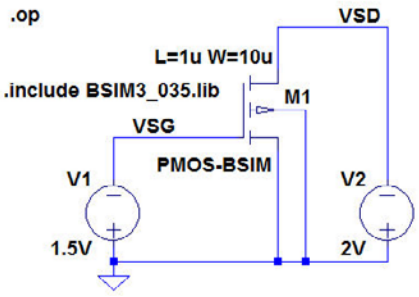
```
.MODEL PMOS-BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.8E-9
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = 150 UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure P3.4

For a PMOS transistor with the transistor model shown in fig. P3.4 (BSIM3 0.35 µm model, fig. 3.10) and channel width $W = 10$ µm and channel length $L = 1$ µm, find the bias current I_D and the small-signal parameters g_m, g_{mb} and g_{ds} in a bias point of $V_{SG} = 1.5$ V, $V_{BS} = 0$ V and $V_{SD} = 2.0$ V. From these small-signal parameters and the bias current, estimate parameters for a Shichman-Hodges model for the transistor. Assume $|2\Phi_F| = 0.7$ V.
Simulate and plot the input characteristics (I_D versus V_{SG}) and output characteristics (I_D versus V_{SD}).

Solution:

The figure below shows the schematic for simulating the small-signal parameters and the resulting error log file with the relevant parameters underlined.

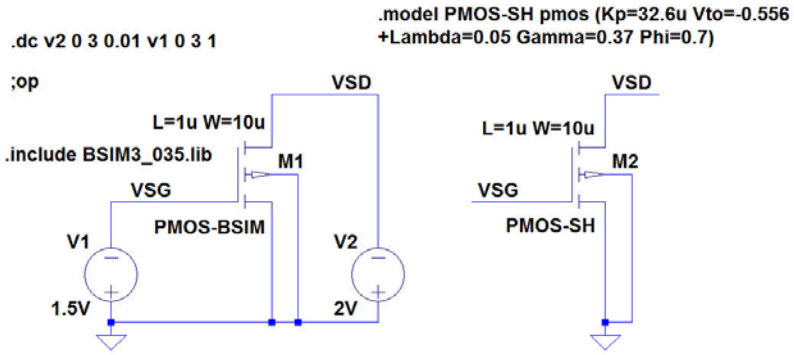



```
Semiconductor Device Operating Points:
                              --- BSIM3 MOSFETS ---

Name:          m1
Model:     pmos-bsim
Id:       -1.60e-04
Vgs:      -1.50e+00
Vds:      -2.00e+00
Vbs:       0.00e+00
Vth:      -6.79e-01
Vdsat:    -6.96e-01
Gm:        3.39e-04
Gds:       7.31e-06
Gmb        7.54e-05
```

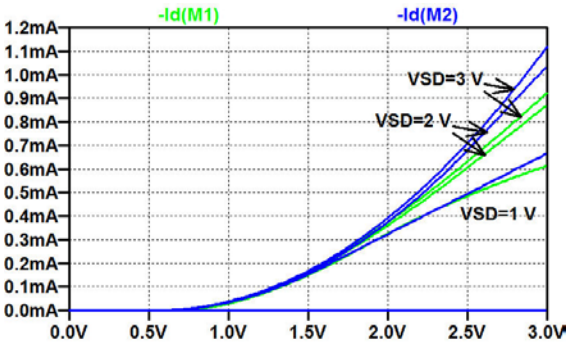
From the small-signal parameters, the following Shichman-Hodges model parameters are calculated. Beware of the signs. For a PMOS transistor, the easiest solution is to use numeric values in the equations (3.12) to (3.15) in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'. Remember that the threshold voltage is negative for a PMOS transistor.

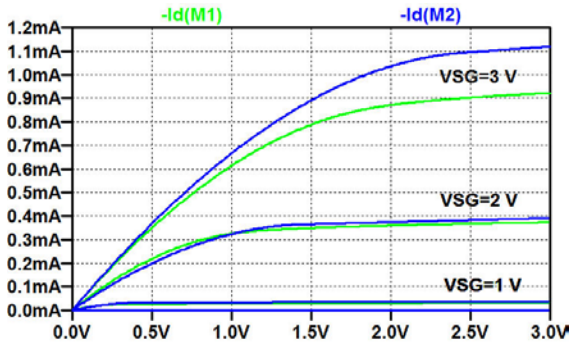
$$\begin{aligned}
\lambda &= \frac{g_{ds}}{|I_D| - g_{ds}|V_{DS}|} = 0.05\ \mathrm{V}^{-1} \\
V_{to} &= -\left(|V_{GS}| - \frac{2\,|I_D|}{g_m}\right) = -0.556\ \mathrm{V} \\
K_p &= \left(\frac{g_m}{|I_D|}\right)^2 \left(\frac{|I_D| - g_{ds}|V_{DS}|}{2(W/L)}\right) = 32.6\ \mu\mathrm{A/V}^2 \\
|2\Phi_F| &= 0.7\ \mathrm{V} \\
\gamma &= 2\sqrt{|2\Phi_F|}\,\frac{g_{mb}}{g_m} = 1.67\,\frac{g_{mb}}{g_m} = 0.37\ \sqrt{\mathrm{V}}
\end{aligned}$$

For simulating the input characteristics and the output characteristics for both the BSIM3 transistor model and the Shichman-Hodges transistor model, the schematic shown below is used. The '.dc' command specification shown gives the output characteristics. For the input characteristics, use `V1` as the first source and `V2` as the second source.



The simulations result in the characteristics shown below with the green curves for the BSIM3 model and the blue curves for the Shichman-Hodges model.





3.5

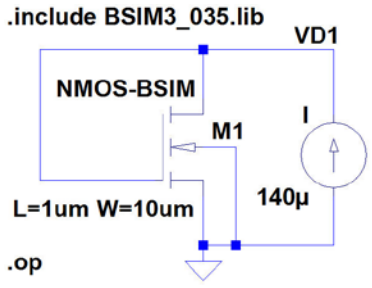
```
.MODEL NMOS-BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = 360 UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03
```

Figure P3.5

For an NMOS transistor with the transistor model shown in fig. P3.5 (BSIM3 0.35 µm model, fig. 3.10), a channel width $W = 10$ µm and channel length $L = 1$ µm, assume a bias point specified by $V_{GS} = V_{DS}$, $V_{SB} = 0$ V and $I_D = 140$ µA. Find g_m, g_{mb} and g_{ds} from a '.op' simulation and estimate parameters K_p, V_{to}, λ and γ for a Shichman-Hodges model for the transistor. Assume $|2\Phi_F| = 0.7$ V.

Solution:

The figure below shows the schematic for simulating the small-signal parameters and the resulting error log file with the relevant parameters underlined.




```
Semiconductor Device Operating Points:
                                --- BSIM3 MOSFETS ---

Name:          m1
Model:     nmos-bsim
Id:         1.40e-04
Vgs:        9.99e-01
Vds:        9.99e-01
Vbs:        0.00e+00
Vth:        5.43e-01
Vdsat:      3.36e-01
Gm:         5.84e-04
Gds:        6.04e-06
Gmb         1.67e-04
```

From the small-signal parameters, the following Shichman-Hodges model parameters are calculated using equations (3.12) to (3.15) in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'.

$$\begin{aligned}
\lambda &= \frac{g_{ds}}{I_D - g_{ds}V_{DS}} = 0.045\ \mathrm{V}^{-1} \\
V_{to} &= V_{GS} - \frac{2\,I_D}{g_m} = 0.520\ \mathrm{V} \\
K_p &= \left(\frac{g_m}{I_D}\right)^2 \left(\frac{I_D - g_{ds}V_{DS}}{2(W/L)}\right) = 117\ \mu\mathrm{A/V}^2 \\
|2\Phi_F| &= 0.7\ \mathrm{V} \\
\gamma &= 2\sqrt{|2\Phi_F|}\,\frac{g_{mb}}{g_m} = 1.67\,\frac{g_{mb}}{g_m} = 0.48\ \sqrt{\mathrm{V}}
\end{aligned}$$

3.6

$K_p = 190\ \mu A/V^2$, $V_{to} = 0.57$ V, $\lambda = 0.16\ V^{-1}$,
$\gamma = 0.5\ \sqrt{V}$, $|2\Phi_F| = 0.7$ V.

Figure P3.6

For an NMOS transistor with the Shichman-Hodges parameters shown in fig. P3.6 and a channel length $L = 1\ \mu m$, simulate and plot g_m and g_{ds} versus the drain current I_D for $W = 10\ \mu m$, $W = 30\ \mu m$ and $W = 50\ \mu m$, and $0 < I_D < 10$ mA. Assume a drain-source voltage of $V_{DS} = 1.2$ V.
From the plots of g_m and g_{ds}, find the maximum drain current for which the transistor is in the active region for each of the three values of channel width.

Solution:

For simulating the small-signal parameters g_m and g_{ds}, we use a circuit similar to the circuit shown in fig. 3.29 in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'. For convenience, fig. 3.29 is shown below.

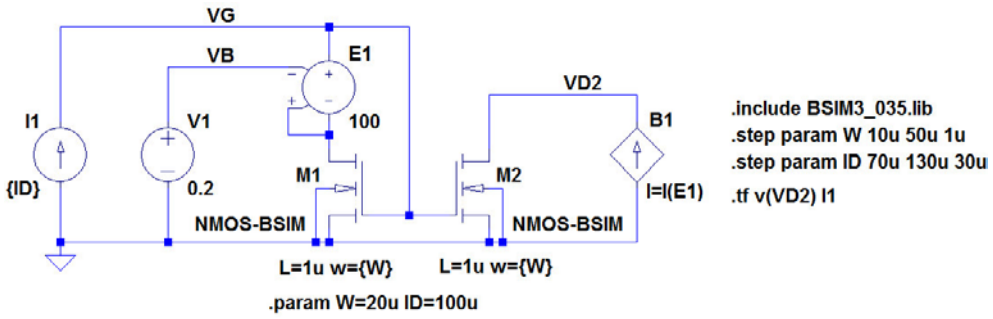


Figure 3.29: NMOS current mirror with voltage buffer for the drain voltage for simulating both g_{ds} and g_m.

The circuit from fig. 3.29 is modified by replacing the controlled current source for M_2 by a constant voltage of 1.2 V in order to obtain a constant V_{DS} for the simulation of g_{ds}. Two '.step param' commands are inserted, one for `ID` and one for `W`. The '.step' command for `ID` is inserted first in order to define `ID` as the first parameter to step, i.e. defining the x-axis in the output plot from the simulation. In order to simulate g_m, we run a '.tf' simulation with `I1` as the source and `v(VG)` as the output, see the figure on the following page. From this simulation, g_m is found as the reciprocal of the input impedance as also shown on the next page. The green curve is for $W = 10\ \mu m$, the blue curve is for $W = 30\ \mu m$, and the red curve is for $W = 50\ \mu m$. Clearly, there is a kink in each of the curves, indicating the limit between

the active region (small values of drain current) and the triode region (large values of drain current).

In the active region, g_m is found from

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D(1+\lambda V_{DS})}$$

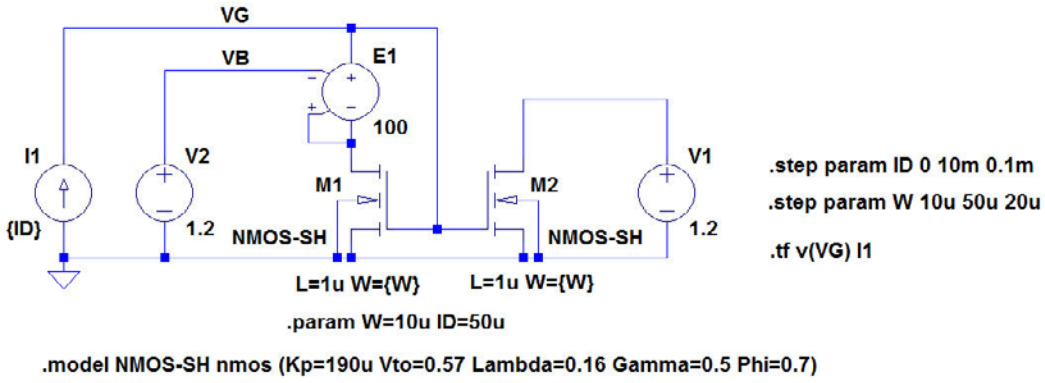
showing a square root dependency on I_D (Equation (3.8) in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide').

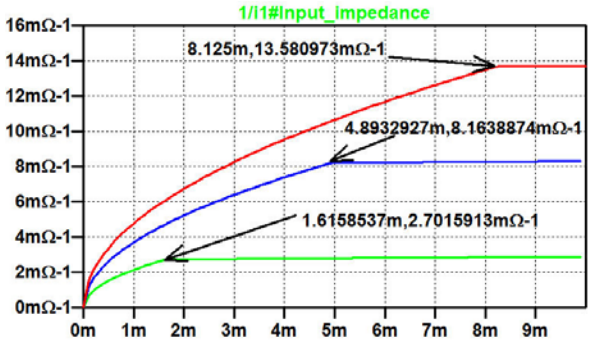
In the triode region, g_m is found from

$$g_m = \mu_n C_{ox}\left(\frac{W}{L}\right) V_{DS}(1+\lambda V_{DS})$$

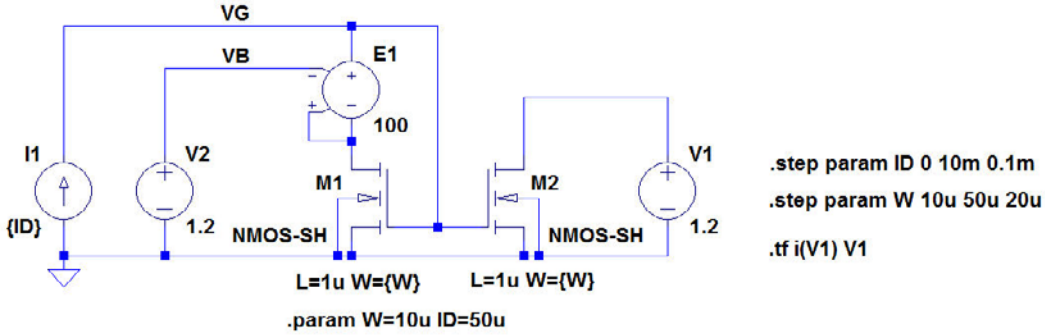
showing that g_m does not depend on I_D (Equation (3.11) in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide').

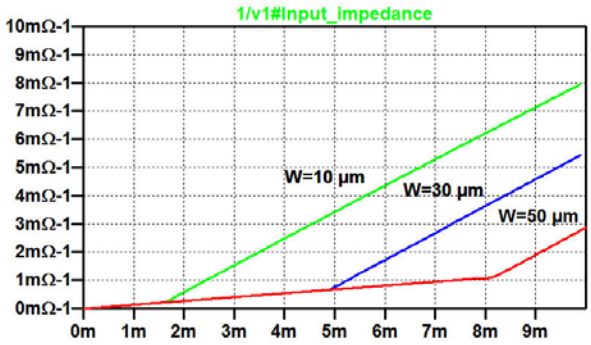
From the kinks, we find the following maximum values of drain current for which the transistor is in the active region:
$W = 10$ µm: $I_{D\max} = 1.62$ mA; $W = 30$ µm: $I_{D\max} = 4.89$ mA; $W = 50$ µm: $I_{D\max} = 8.13$ mA.





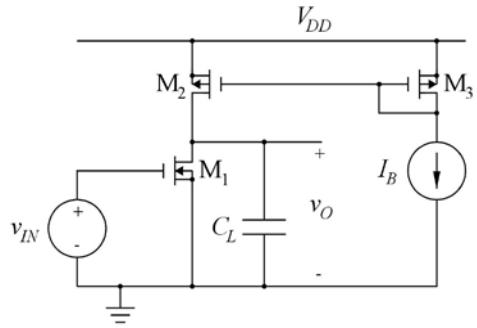
In order to simulate g_{ds}, we run a '.tf' simulation with `V1` as the source and `i(V1)` as the output, see the figure below. From this simulation, g_{ds} is found as the reciprocal of the input impedance as shown below. Again, clear kinks are seen, indicating the limit between the active region and the triode region.





Tutorial 4 – Basic Gain Stages

4.1



$W_2 = W_3 = 25$ µm, $L_1 = L_2 = L_3 = 1$ µm
$C_L = 3.2$ pF, $V_{DD} = 3$ V, $I_B = 100$ µA.

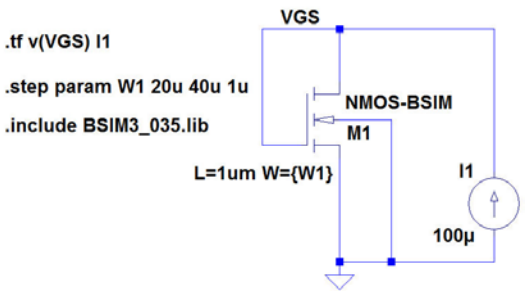
Figure P4.1

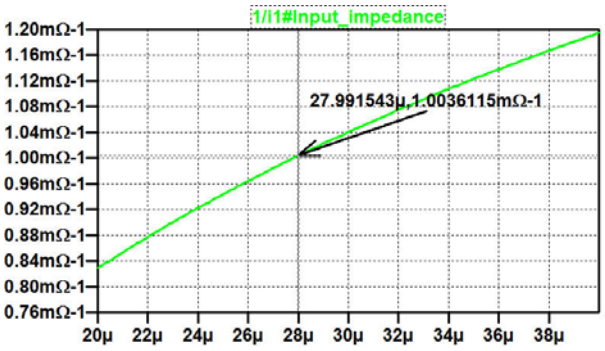
For the common-source amplifier shown in fig. P4.1, design M_1 so that the gain-bandwidth product of the stage is 50 MHz. Assume a transistor model as specified in fig. P3.2 on page 98 and fig. P3.3 on page 99 and use a channel length of $L_1 = 1$ µm. Use a channel width for M_1 which is a multiple of 1 µm.
Hint: Design M_1 to have the required g_m for the gain-bandwidth product with $I_D = 100$ µA. Find g_m versus I_D using the method shown in example 3.5 on page 90.
Find the dc bias value of the input voltage for which the output voltage is 1.5 V and find the small-signal voltage gain A_v at low frequencies.

Figs. P3.2 and P3.3 are shown on page 31 and 33, respectively, in this book.

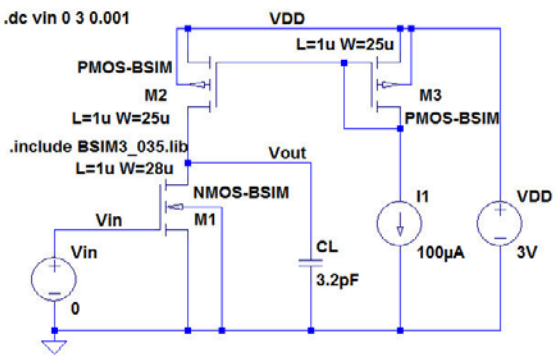
Solution:

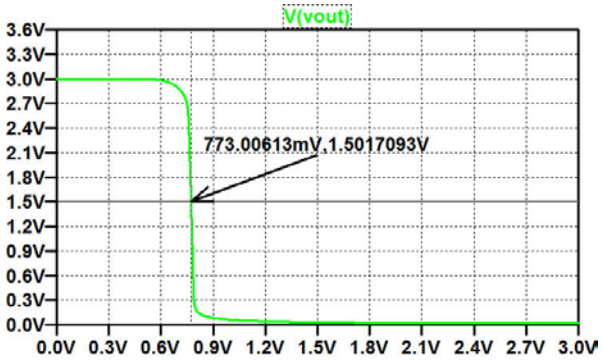
From $2\pi GBW = g_{m1}/C_L$, we find $g_{m1} = 1.0$ mA/V. In order to find a transistor channel width giving this value of g_m, we run the simulation shown below. From this, we find $W_1 = 28$ µm.



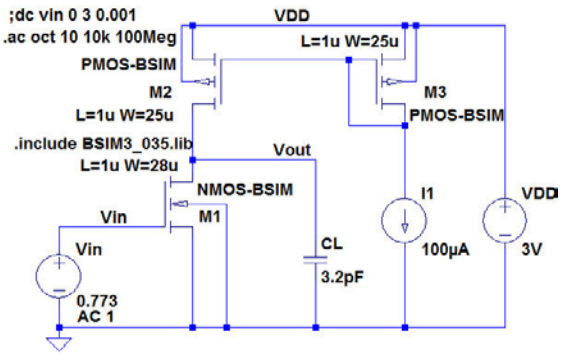


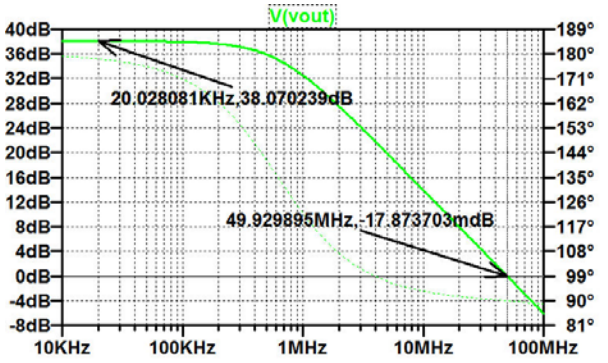
With $W_1 = 28$ µm, the common-source amplifier is shown in the figure below with a specification for a '.dc' simulation. From the resulting simulation, we find an input bias voltage of $V_{IN} = 0.773$ V for an output bias voltage of 1.5 V.



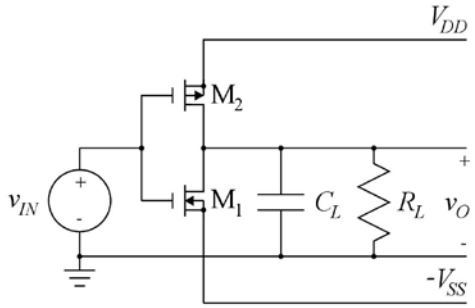


With the bias value for `Vin` inserted and with an ac amplitude of 1 V for `Vin`, a '.ac' simulation will show both the gain at low frequencies and verify the gain-bandwidth product of 50 MHz. The figures below show the schematic and the resulting simulation plot. From the plot, we find a low-frequency gain of 38 dB and a gain-bandwidth product of 50 MHz, found as the frequency where the gain has dropped to 0 dB.





4.2



$V_{DD} = V_{SS} = 1.5$ V, $L_1 = L_2 = 1$ µm
$C_L = 0.5$ pF, $R_L = 10$ kΩ

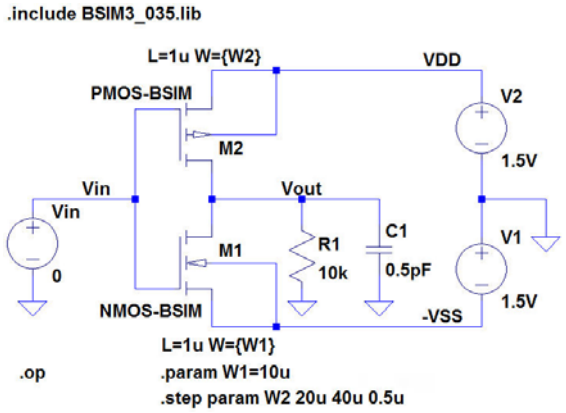
Figure P4.2

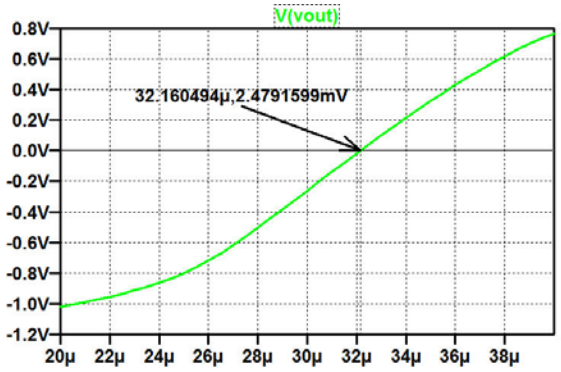
For the inverting amplifier shown in fig. P4.2, design M_1 and M_2 so that the dc bias value of the output voltage is within the range ±100 mV with an input dc bias voltage of 0 V and so that the low-frequency small-signal gain with an input dc bias voltage of 0 V is −10 V/V. Assume transistor models as specified in fig. P3.2 on page 98 and fig. P3.3 on page 99 and use a channel length of $L_1 = L_2 =$ 1 µm. Use channel widths for M_1 and M_2 which are multiples of 0.5 µm. What is the low-frequency small-signal gain if the load resistor R_L is omitted? What is the gain-bandwidth product of the amplifier for $R_L = 10$ kΩ and for $R_L = \infty$?

Figs. P3.2 and P3.3 are shown on page 31 and 33, respectively in this book.

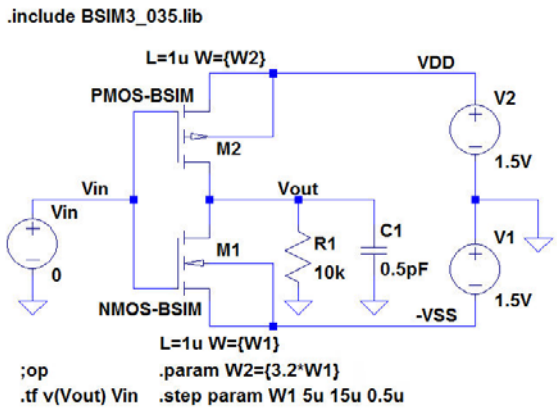
Solution:

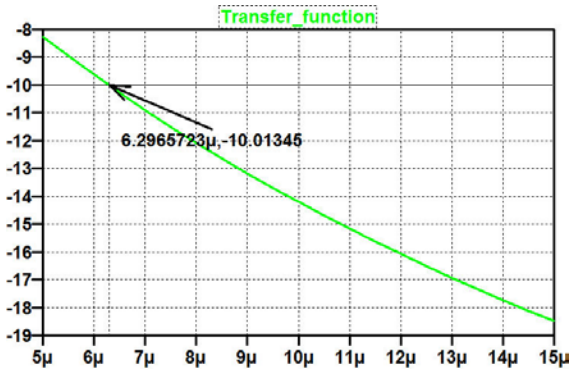
We start the solution by finding a ratio between the channel widths for the NMOS transistor (M_1) and the PMOS transistor (M_2). For this, we may run a simulation as shown below where the channel widths are defined as parameters. The width W_1 is selected to be 10 µm while the width W_2 is stepped from $2\,W_1$ (20 µm) to $4\,W_1$ (40 µm). From a '.op' simulation, the output voltage is plotted versus W_2. The plot below shows that with $W_1 = 10$ µm, W_2 should be 32 µm in order to obtain an output voltage of 0 V. Thus, the ratio between W_2 and W_1 is 3.2.





Next, we define the parameter `W2` to be 3.2 times the parameter `W1` and we step the parameter `W1` over a suitable range (5 µm to 15 µm) and run a '.tf' simulation in order to find the low-frequency gain as a function of W_1, see figures below. From the simulation plot, we find that in order to obtain a gain of -10 V/V, W_1 should be 6.3 µm. Nearest multiple of 0.5 µm is $W_1 = 6.5$ µm, and with this value of W_1, we find $W_2 = 3.2\,W_1 = 20.8$ µm. Rounding off to nearest multiple of 0.5 µm gives $W_2 = 21$ µm.





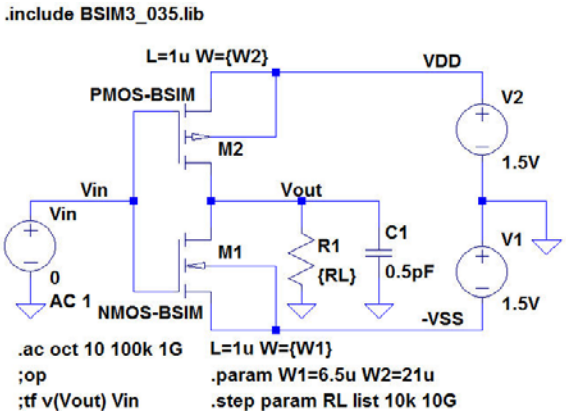
With $W_1 = 6.5$ µm and $W_2 = 21$ µm, we run a '.op' simulation to verify the bias value of the output voltage and a '.tf' simulation to verify the gain.

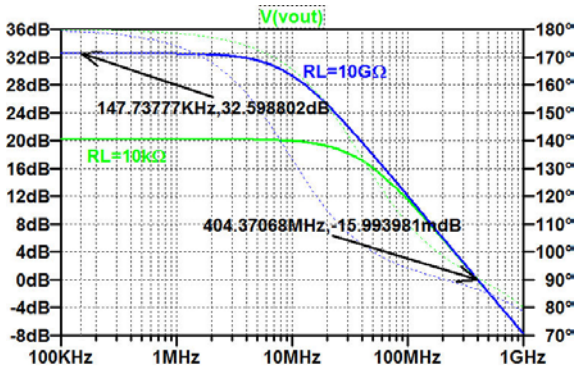
The outputs of these simulations are shown below, and we find results reasonably close to the design targets.

```
        --- Operating Point ---

V(vout):        0.0203095       voltage
V(vin):         0               voltage
V(vdd):         1.5             voltage
V(-vss):        -1.5            voltage
```

```
        --- Transfer Function ---

Transfer_function:              -10.2859        transfer
vin#Input_impedance:            1e+020          impedance
output_impedance_at_V(vout):    7651.2          impedance
```

Finally, in order to find low-frequency gain and gain-bandwidth product for $R_L = 10$ kΩ and $R_L = \infty$, we run a '.ac' simulation with R_L stepped between two values, 10k and 10G. From the simulation plot on the following page, we find that with $R_L = \infty$ (10G), the low-frequency gain is 32.6 dB (or -43.6 V/V), and the gain-bandwidth product is 404 MHz, independent of R_L.

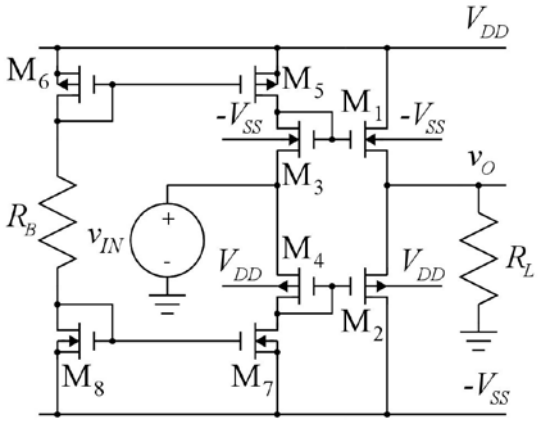




In order to verify that the '.ac' simulation runs from a reasonable bias point, also when $R_L = \infty$, a '.op' simulation with `RL=10G` may be run. The output file from this simulation is shown below, confirming that the bias value of V_O is less than 100 mV.

```
        --- Operating Point ---

V(vout):        0.0856978       voltage
V(vin):         0               voltage
V(vdd):         1.5             voltage
V(-vss):        -1.5            voltage
```

4.3



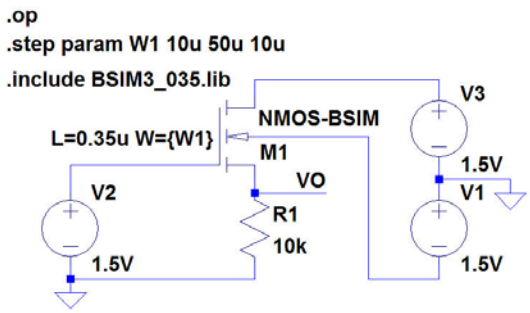
$L_1 = L_2 = L_3 = L_4 = L_5 = L_6 = L_7 = L_8 = 0.35$ μm
$R_L = 10$ kΩ, $V_{DD} = V_{SS} = 1.5$ V.

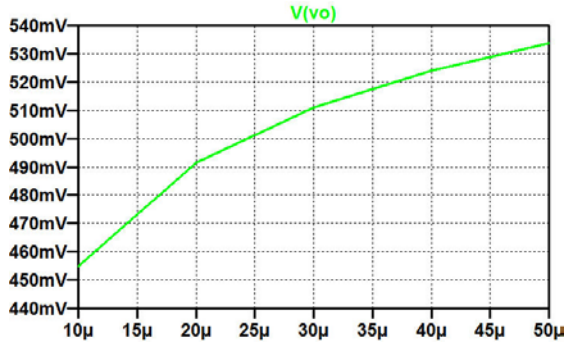
Figure P4.3

Fig. P4.3 shows a class AB buffer amplifier. Design the output transistors M_1 and M_2 so that the amplifier can deliver an output voltage swing of ± 0.5 V with a load resistor of 10 kΩ. Assume that the gate voltage of M_1 and M_2 can reach the positive and negative supply voltages, respectively. Select values of the channel widths which are multiples of 10 μm. Use transistor models as specified in fig. P3.2 on page 98 and fig. P3.3 on page 99. Design the bias network M_3 - M_8 and R_B to provide a bias current of 1 μA for M_3 - M_8. M_5 - M_8 should be designed to have a saturation voltage $|V_{DS\text{sat}}|$ of less than 50 mV, and the channel widths should be multiples of 10 μm. M_3 and M_4 should be scaled to channel widths of 0.1 times the channel widths of M_1 and M_2, respectively.
Plot the output voltage versus the input voltage for -1.5 V $< v_{IN} <$ 1.5 V. Find the open circuit voltage gain and the output resistance of the buffer for an input bias voltage of 0 V. Find the bias current in M_1 and M_2 for an output bias voltage of $V_O = 0$ V. Why is the current scaling in M_1 - M_2 / M_3 - M_4 different from the channel width scaling?

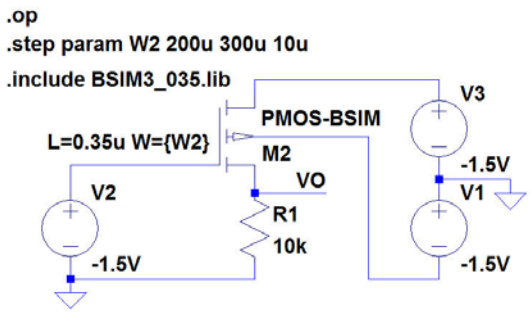
Solution:

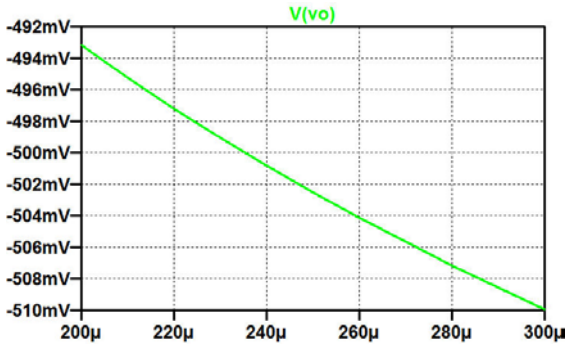
For finding the channel width W_1, we run a '.op' simulation on a single NMOS transistor with gate, source, drain and bulk connected to voltages resulting in the highest value of output voltage. Using a '.step param' directive, the output voltage is simulated versus the channel width. The figure below shows the schematic and the simulation plot from which we find $W_1 = 30$ µm (using multiples of 10 µm) in order to achieve an output voltage of +0.5 V.





The channel width W_2 is found in the same way as W_1, running a '.op' simulation on a single PMOS transistor with gate, source, drain and bulk connected to voltages resulting in the lowest value of output voltage. The figure below shows the schematic and the simulation plot from which we find $W_2 = 240$ µm (using multiples of 10 µm) in order to achieve an output voltage of -0.5 V.

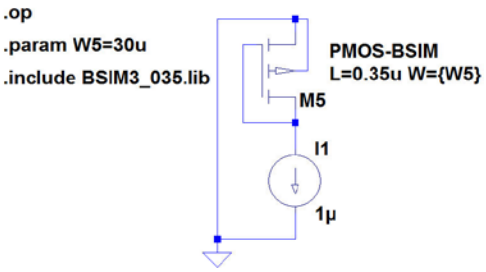




For the bias network, M_3 and M_4 are designed by scaling W_1 and W_2 by a factor of 10, respectively. This gives $W_3 = 3$ µm and $W_4 = 24$ µm.

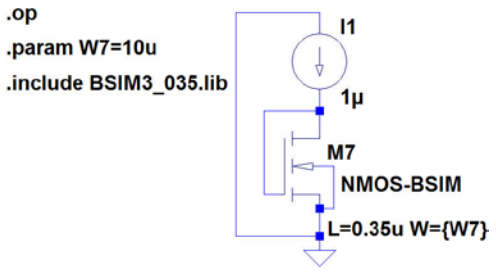
The transistors M_5 - M_8 should have a saturation voltage of less than 50 mV for a drain current of 1 µA.

For the PMOS transistors (M_5 and M_6), the channel width is found from the simulation shown in the figure below. The simulation is run with different values of `W5` in multiples of 10 µm and the smallest value of `W5` resulting in $|$`Vdsat`$| < 50$ mV is selected, i.e. $W_5 = W_6 = 30$ µm.



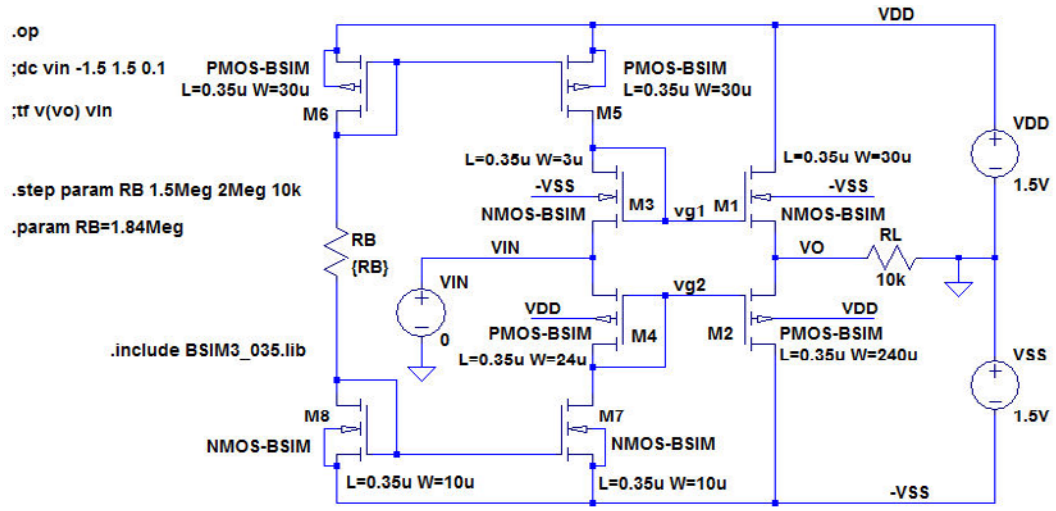

```
Semiconductor Device Operating Points:
                              --- BSIM3 MOSFETS ---
Name:         m5
Model:     pmos-bsim
Id:       -1.00e-06
Vgs:      -6.25e-01
Vds:      -6.25e-01
Vbs:       0.00e+00
Vth:      -7.26e-01
Vdsat:    -4.87e-02
```

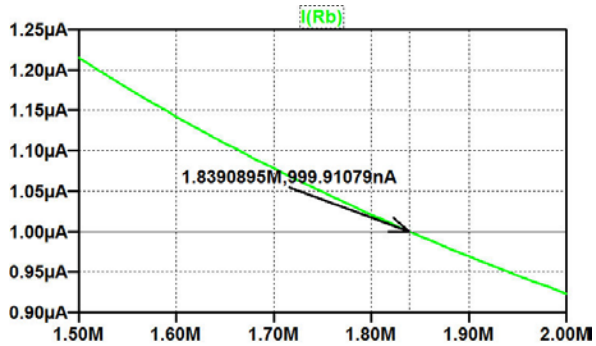
For the NMOS transistors (M_7 and M_8), the channel width is found from the simulation shown in the figure below. The simulation is run with different values of `W7` in multiples of 10 µm and the smallest value of `W7` resulting in `Vdsat` < 50 mV is selected, i.e. $W_7 = W_8 = 10$ µm.



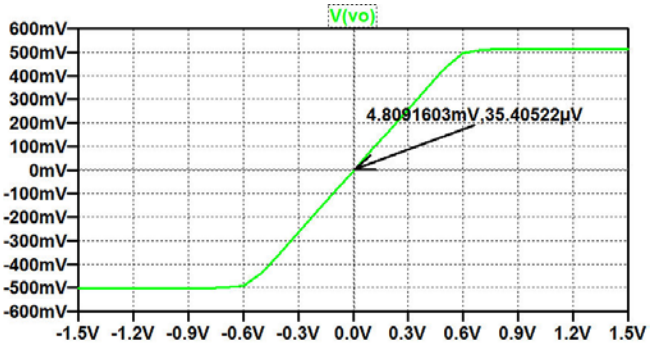

```
Semiconductor Device Operating Points:
                                --- BSIM3 MOSFETS ---
Name:          m7
Model:      nmos-bsim
Id:          1.00e-06
Vgs:         5.36e-01
Vds:         5.36e-01
Vbs:         0.00e+00
Vth:         5.63e-01
Vdsat:       4.41e-02
```

With all transistor dimensions in place, the complete schematic can be drawn as shown below. The only device still to be designed is R_B. This can be found from a '.op' simulation with `RB` stepped over a suitable range. From the simulation plot shown below, we find $R_B = 1.84$ MΩ.





Next, a '.dc' simulation is run, resulting in the simulation plot shown below. For this simulation, the '.step param' directive is changed into a comment and R_B is defined by the '.param' command shown in the schematic on the previous page.



For finding the open circuit voltage gain and output resistance for an input bias voltage of 0 V, we run a '.tf' simulation with RL disconnected. The output file is shown below, and we find $A_{vo\mathrm{c}} = 0.95$ V/V and $r_o = 1005\ \Omega$.

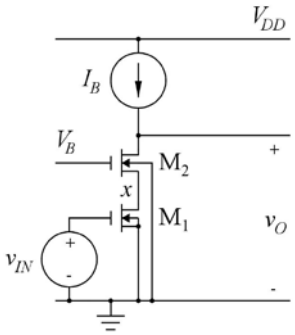
```
       --- Transfer Function ---

Transfer_function:            0.951633       transfer
vin#Input_impedance:          674020         impedance
output_impedance_at_V(vo):    1005.47        impedance
```

For finding the bias currents in M_1 and M_2 for an output voltage of 0 V, we use the '.dc' simulation shown on the previous page to find the value of the input voltage resulting in V(vo) = 0. From the plot, we find an input voltage of 4.809 mV. With this value of VIN, we run a '.op' simulation, and the error log file from this gives all the transistor bias currents as shown below.

```
Semiconductor Device Operating Points:
                          --- BSIM3 MOSFETS ---
Name:         m6           m5           m2           m4           m8
Model:     pmos-bsim    pmos-bsim    pmos-bsim    pmos-bsim    nmos-bsim
Id:       -9.99e-07    -1.01e-06    -1.89e-05    -1.05e-06     9.99e-07
Vgs:      -6.25e-01    -6.25e-01    -8.82e-01    -8.86e-01     5.36e-01
Vds:      -6.25e-01    -6.35e-01    -1.50e+00    -8.86e-01     5.36e-01
Vbs:       0.00e+00     0.00e+00     1.50e+00     1.50e+00     0.00e+00
Vth:      -7.26e-01    -7.26e-01    -9.53e-01    -9.77e-01     5.63e-01
Vdsat:    -4.87e-02    -4.87e-02    -5.94e-02    -5.54e-02     4.41e-02

Name:         m7           m3           m1
Model:     nmos-bsim    nmos-bsim    nmos-bsim
Id:        1.05e-06     1.01e-06     1.89e-05
Vgs:       5.36e-01     8.60e-01     8.65e-01
Vds:       6.18e-01     8.60e-01     1.50e+00
Vbs:       0.00e+00    -1.50e+00    -1.50e+00
Vth:       5.62e-01     8.45e-01     8.32e-01
Vdsat:     4.43e-02     5.94e-02     6.62e-02
```

Obviously, the current scaling in M_1 - M_2 / M_3 - M_4 is larger than the channel width scaling. This is caused by the larger $|V_{DS}|$ values for M_1 - M_2 than for M_3 - M_4, by the input offset voltage, and by the smaller threshold voltages for M_1 - M_2 than for M_3 - M_4.

4.4



$L_1 = L_2 = 1$ µm, $W_1 = W_2 = 10$ µm
$I_B = 20$ µA, $V_B = 1.5$ V, $V_{DD} = 3$ V.

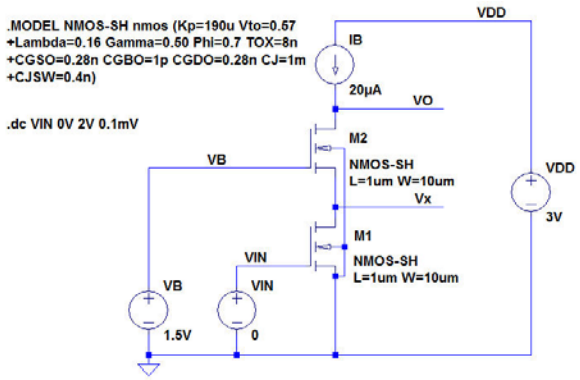
.MODEL NMOS-SH nmos (Kp=190u Vto=0.57
+Lambda=0.16 Gamma=0.50 Phi=0.7 TOX=8n
+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m
+CJSW=0.4n)

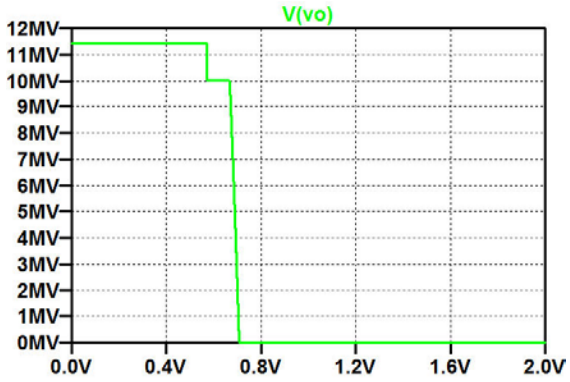
Figure P4.4

For the telescopic cascode shown in fig. P4.4, find the bias value of V_{IN} required to give an output voltage of 2 V. Also find the small-signal gain A_{voc} and output resistance r_o at low frequencies. Find the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1. Assume a transistor model as shown in fig. P4.4.

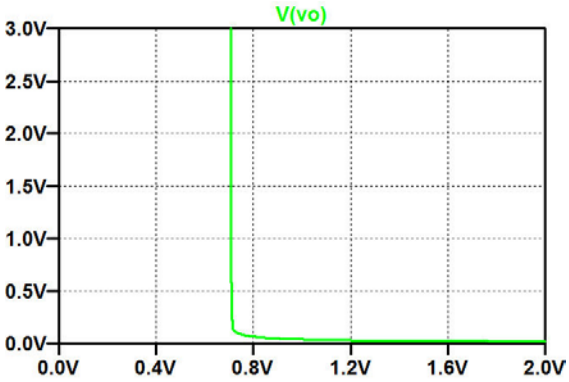
Solution:

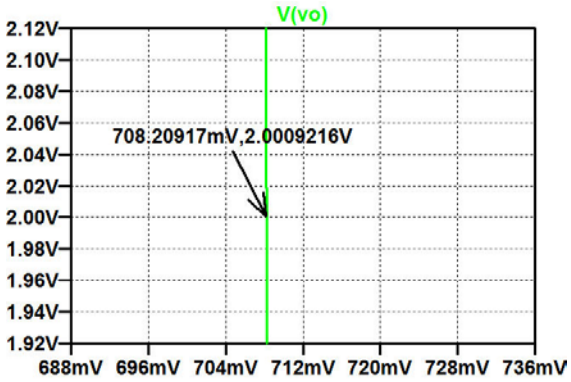
The figure below shows the cascode stage with a specification for a '.dc' simulation. Also shown is the resulting plot of the output voltage. Obviously, the simulation generates unrealistically high output voltages, several MV. This is due to the fact that the drain of M_2 is connected directly to an ideal dc current source.





In order to see `V(vo)` in a realistic range of output voltages, we set the range of the y-axis to 3 V, either by the command 'Plot Settings → Manual Limits' or by moving the cursor to the y-axis and using a left click on the mouse. The resulting plot is shown below, left plot. Obviously, the output voltage changes abruptly for an input voltage of about 0.7 V, and in order to find the exact input voltage, we zoom in on a small part of the plot, see right plot below. From this, we find $V_{IN} = 708.21$ mV. Notice that this value has been specified with a resolution exceeding the step size in the '.dc' command, so it is based on an interpolation.





In order to verify the bias point, we run a '.op' simulation with a dc value of V_{IN} specified to 708.21 mV. The output file from this is shown below, and we see that `V(vo)` is sufficiently close to 2 V.

```
        --- Operating Point ---

V(vx):          0.638226        voltage
V(vin):         0.70821         voltage
V(vo):          1.97479         voltage
V(vb):          1.5             voltage
V(vdd):         3               voltage
```

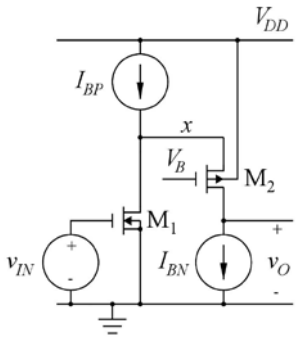
With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a '.tf' simulation with `V(VO)` as the output and `VIN` as the source. The output file from this '.tf' simulation is shown below. From this, we find a gain of -14065 V/V or 83 dB and an output resistance of 49 MΩ.

```
        --- Transfer Function ---

Transfer_function:              -14065.1        transfer
vin#Input_impedance:            1e+020          impedance
output_impedance_at_V(vo):      4.89777e+007    impedance
```

For finding the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1, we run a '.tf' simulation with `V(Vx)` as the output and `VIN` as the source. The output file from this '.tf' simulation is shown below. From this, we find a resistance r_x of 344 kΩ.

```
        --- Transfer Function ---

Transfer_function:              -99.6727        transfer
vin#Input_impedance:            1e+020          impedance
output_impedance_at_V(vx):      344394          impedance
```

4.5



$L_1 = L_2 = 1$ µm, $W_1 = 10$ µm, $W_2 = 30$ µm
$I_{BP} = 40$ µA, $I_{BN} = 20$ µA, $V_B = 1.5$ V, $V_{DD} = 3$ V.

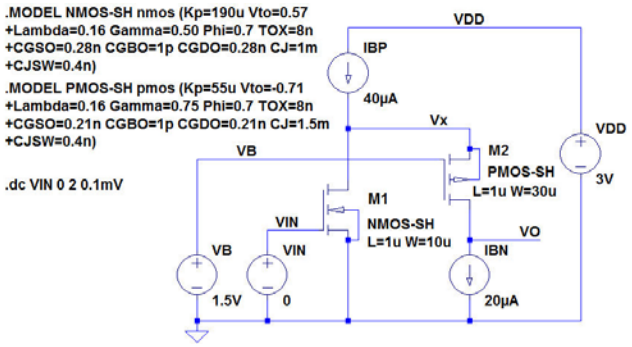
.MODEL PMOS-SH pmos (Kp=55u Vto=-0.71
+Lambda=0.16 Gamma=0.75 Phi=0.7 TOX=8n
+CGSO=0.21n CGBO=1p CGDO=0.21n CJ=1.5m
+CJSW=0.4n)

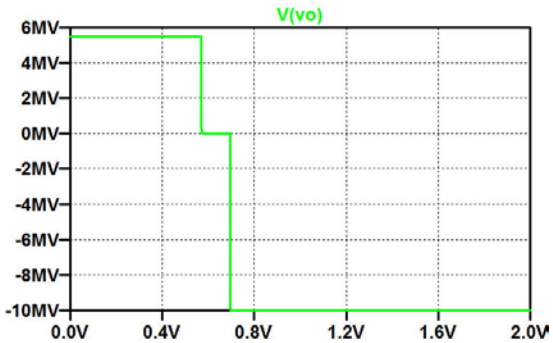
Figure P4.5

For the folded cascode shown in fig. P4.5, find the bias value of V_{IN} required to give an output voltage of 1 V. Also find the small-signal gain A_{voc} and output resistance r_o at low frequencies. Find the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1. Assume transistor models as shown in fig. P4.4 and P4.5.

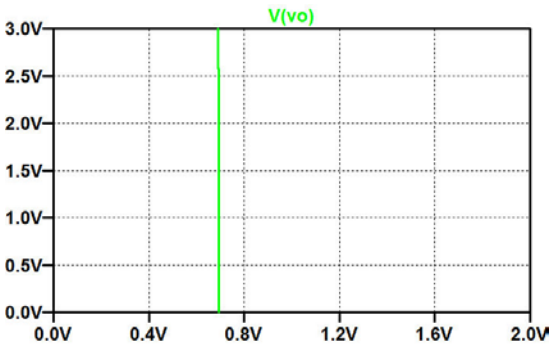
Solution:

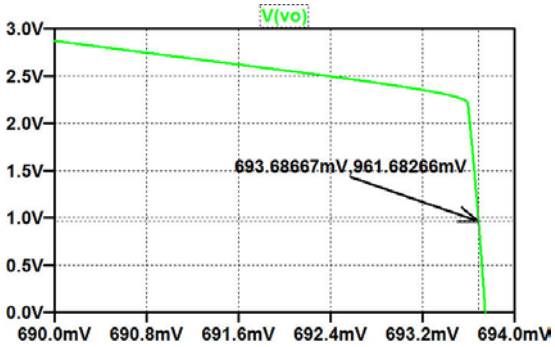
The figure below shows the folded-cascode stage with a specification for a '.dc' simulation. Also shown is the resulting plot of the output voltage. Obviously, the simulation generates unrealistically high output voltages, several MV. This is due to the biasing by two ideal dc current sources. You may also notice that the simulation time is quite long, and examining the error log file, you find that LTspice has some challenges in finding the operating points for the values of input voltage giving unrealistic values of output voltage.





In order to see `V(vo)` in a realistic range of output voltages, we set the range of the y-axis to 3 V, either by the command 'Plot Settings → Manual Limits' or by moving the cursor to the y-axis and using a left click on the mouse. The resulting plot is shown below, left plot. Obviously, the output voltage changes abruptly for an input voltage of about 0.7 V. Even when zooming in on a small part of the plot, it is difficult to find the value of V_{IN} resulting in an output voltage of 1 V, so in order to improve the accuracy, we run a '.dc' simulation from 690 mV to 694 mV with a step size of 1 µV. From this, we find $V_{IN} = 693.687$ mV.





In order to verify the bias point, we run a '.op' simulation with a dc value of V_{IN} specified to 693.687 mV. The output file from this is shown below, and we see that `V(vo)` is sufficiently close to 1 V, and also the voltage at the intermediate node x has a reasonable value within the supply voltage range.

```
      --- Operating Point ---

V(vx):          2.35079       voltage
V(vin):         0.693687      voltage
V(vdd):         3             voltage
V(vb):          1.5           voltage
V(vo):          0.95661       voltage
```

With the bias point in place, the small-signal gain A_{voc} and output resistance r_o at low frequencies are found from a '.tf' simulation with `V(VO)` as the output and `VIN` as the source. The output file from this '.tf' simulation is shown below. From this, we find a gain of -15241 V/V or 84 dB and an output resistance of 48 MΩ.

```
      --- Transfer Function ---

Transfer_function:            -15241.3       transfer
vin#Input_impedance:          1e+020         impedance
output_impedance_at_V(vo):    4.7511e+007    impedance
```

For finding the small-signal resistance r_x to ground from the node x between the source of M_2 and the drain of M_1, we run a '.tf' simulation with `V(Vx)` as the output and `VIN` as the source. The output file from this '.tf' simulation is shown below. From this, we find a resistance r_x of 430 kΩ.

```
      --- Transfer Function ---

Transfer_function:            -139.073       transfer
vin#Input_impedance:          1e+020         impedance
output_impedance_at_V(vx):    430039         impedance
```

4.6

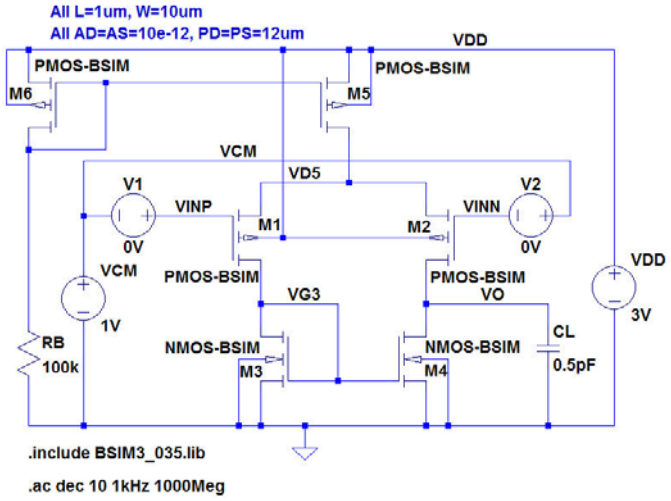


Figure P4.6

Fig. P4.6 shows an alternative version of the LTspice schematic from fig. 4.21 with a different arrangement for the input voltages. Define the ac amplitudes of `VCM`, `V1`, `V2` and `VDD` such that the '.ac' simulation shows the differential gain and compare your simulation to fig. 4.25. Next, define the ac amplitudes of `VCM`, `V1`, `V2` and `VDD` such that the '.ac' simulation shows the common-mode gain and compare your simulation to fig. 4.26. Finally, define the ac amplitudes of `VCM`, `V1`, `V2` and `VDD` such that the '.ac' simulation shows the power supply rejection and compare your simulation to fig. 4.27.

For convenience, fig. 4.21 is shown below.

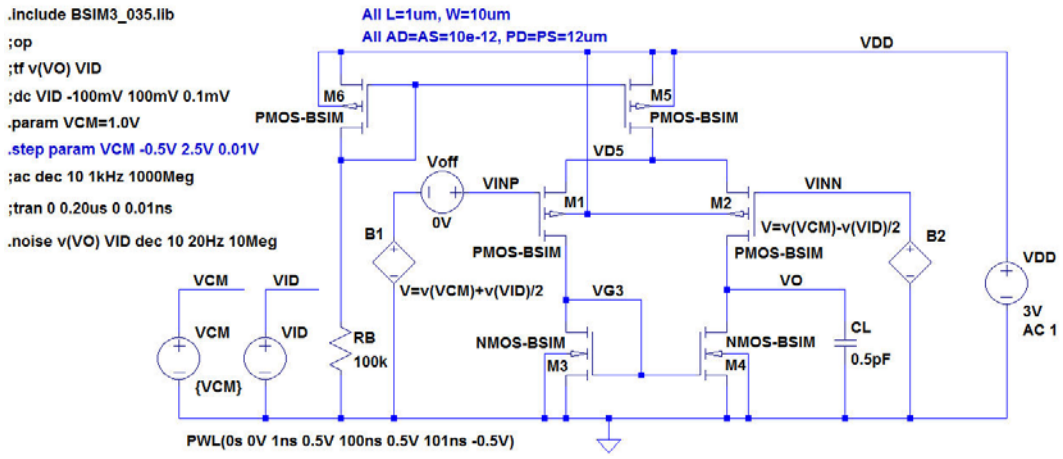
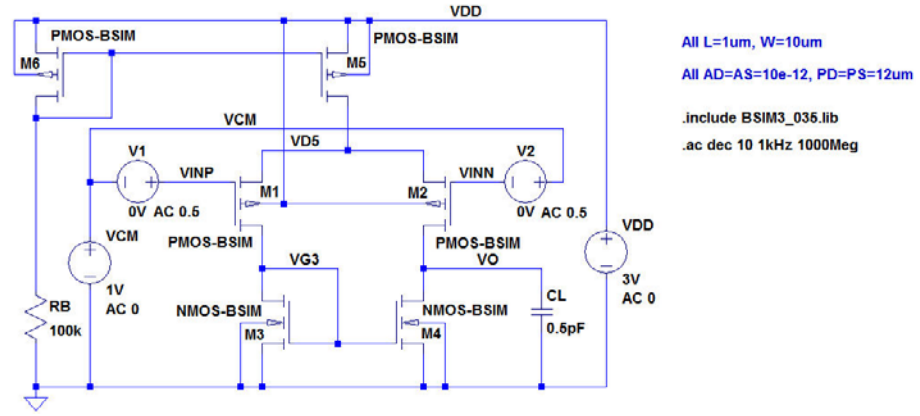
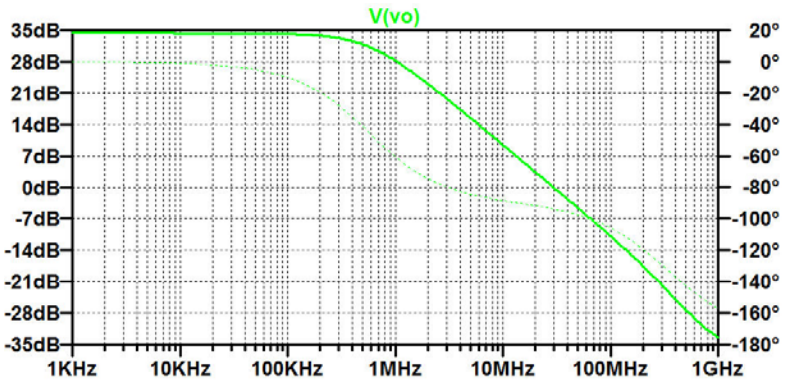


Figure 4.21: LTspice schematic for simulations of a PMOS differential pair with NMOS active load.

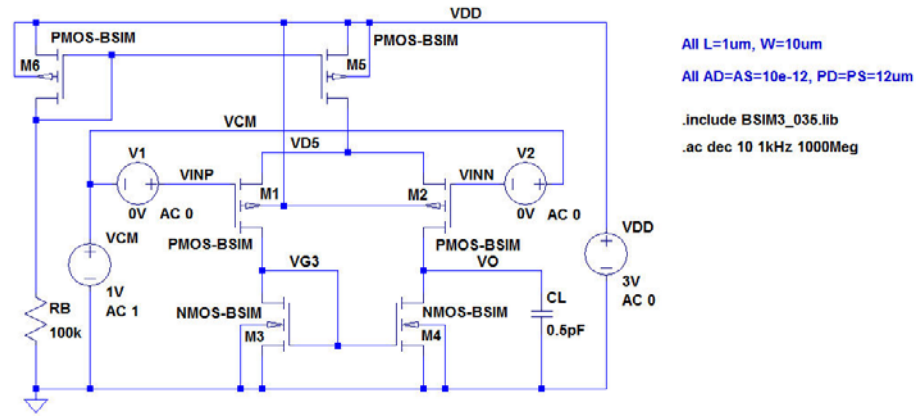
Solution:

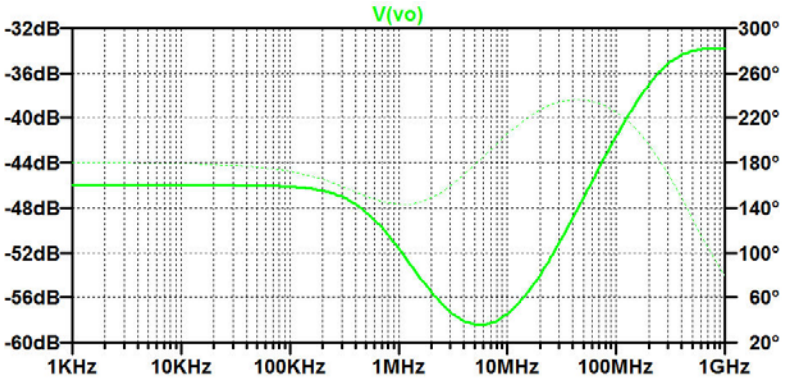
For the differential gain, we define the ac amplitudes in fig. P4.6 as follows:
`VCM`: AC Amplitude = 0, `V1`: AC Amplitude = 0.5, `V2`: AC Amplitude = 0.5, `VDD`: AC Amplitude = 0.
The resulting schematic and simulation plot is shown below. The simulation plot is identical to fig. 4.25 in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'.



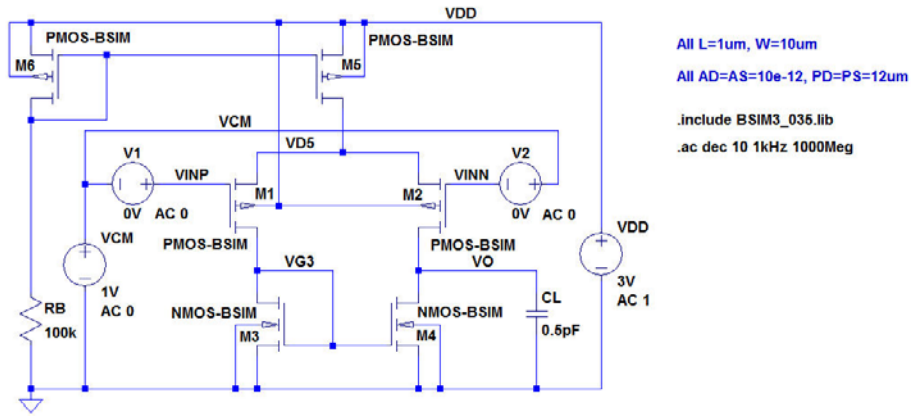


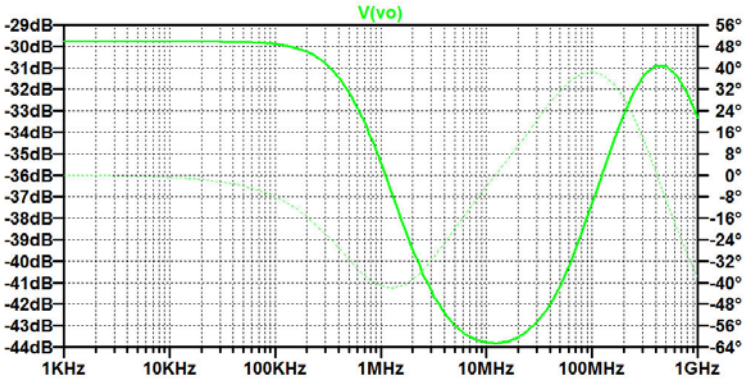
For the common-mode gain, we define the ac amplitudes in fig. P4.6 as follows:
VCM: AC Amplitude = 1, V1: AC Amplitude = 0, V2: AC Amplitude = 0, VDD: AC Amplitude = 0.
The resulting schematic and simulation plot is shown below. The simulation plot is identical to fig. 4.26 in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'.



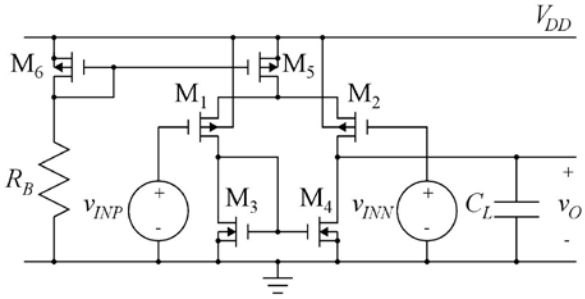


For the power supply rejection, we define the ac amplitudes in fig. P4.6 as follows:
VCM: AC Amplitude = 0, V1: AC Amplitude = 0, V2: AC Amplitude = 0, VDD: AC Amplitude = 1.
The resulting schematic and simulation plot is shown below. The simulation plot is identical to fig. 4.27 in 'CMOS Integrated Circuit Simulation with LTspice – a Tutorial Guide'.





4.7



$L_1 = L_2 = L_3 = L_4 = L_5 = 1$ µm

$W_1 = 30$ µm, $W_2 = 33$ µm, $W_3 = W_4 = W_5 = W_6 = 10$ µm

$AD_1 = AS_1 = AD_2 = AS_2 = 30\ (\mu m)^2$

$AD_3 = AS_3 = AD_4 = AS_4 = AD_5 = AS_5 = AD_6 = AS_6 = 10\ (\mu m)^2$

$PD_1 = PS_1 = PD_2 = PS_2 = 32$ µm

$PD_3 = PS_3 = PD_4 = PS_4 = PD_5 = PS_5 = PD_6 = PS_6 = 12$ µm

$R_B = 100$ kΩ, $C_L = 0.5$ pF, $V_{DD} = 3.0$ V, $V_{CM} = 1$ V

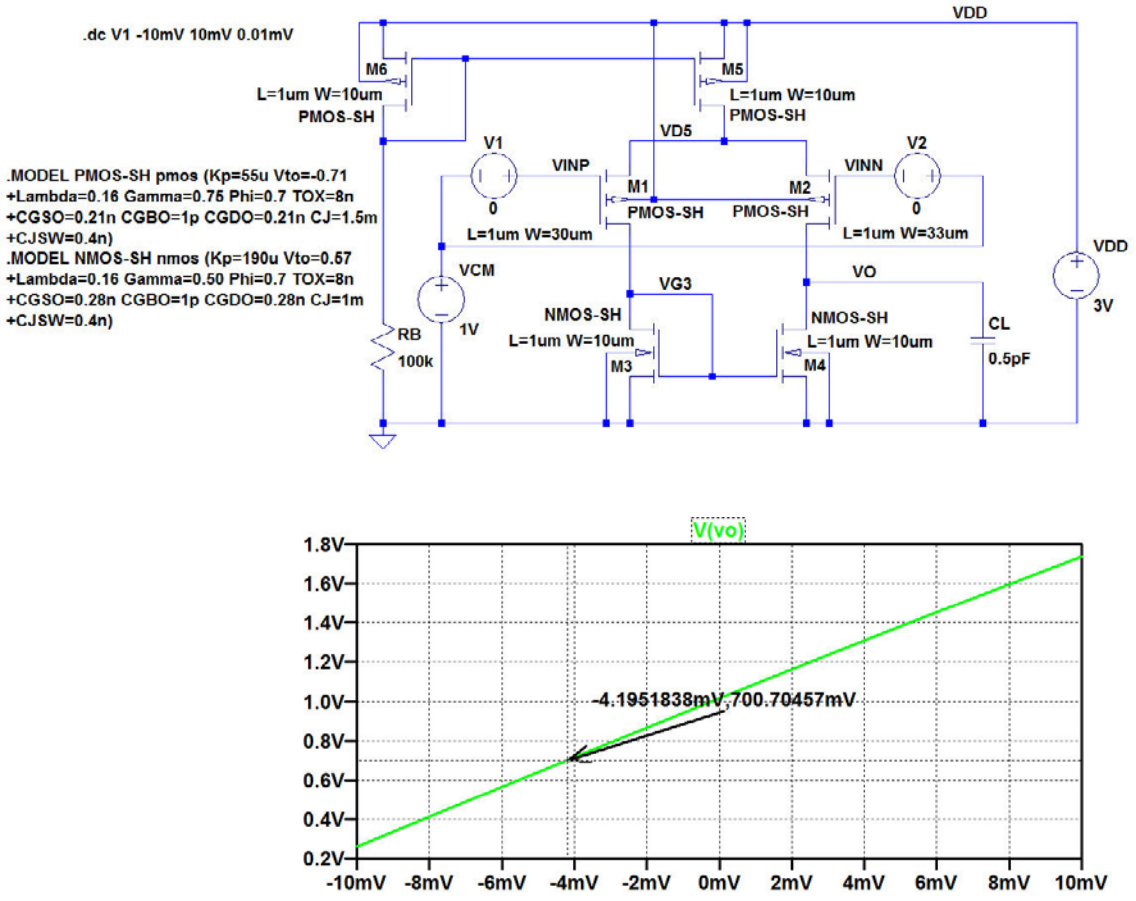
Figure P4.7

For the differential pair shown in fig. P4.7, we assume that a layout error has resulted in a mismatch between M_1 and M_2 such that $W_1 = 30$ µm and $W_2 = 33$ µm. Find the input offset voltage caused by this error for a common-mode input voltage of $V_{CM} = 1$ V and an output voltage of 0.7 V. Use the Shichman-Hodges transistor model from fig. P4.4 and P4.5. Next, plot the differential gain and the common-mode gain versus frequency. Find the gain-bandwidth product and calculate the common-mode rejection ratio at low frequencies. Also plot the gain from the power supply to the output and calculate the power supply rejection ratio at low frequencies.

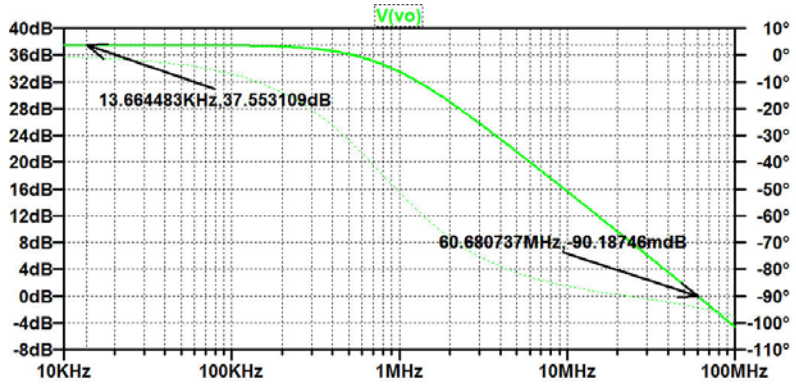
Figs. P4.4 and P4.5 are shown on page 55 and 58, respectively, in this book.

Solution:

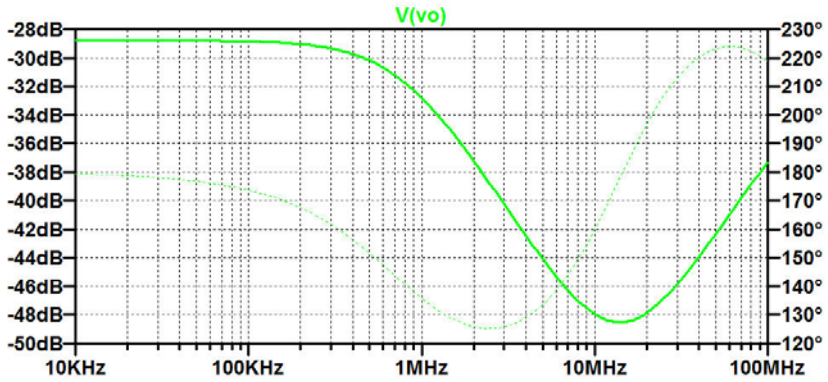
The figure below shows the schematic in LTspice. For finding the offset voltage, we use a '.dc' simulation with the input voltage V1 to the noninverting input as the source to sweep. From the simulation plot below, we find that a dc input voltage of -4.2 mV results in an output voltage of 0.7 V. Thus, $V_{\text{off}} = -4.2$ mV.



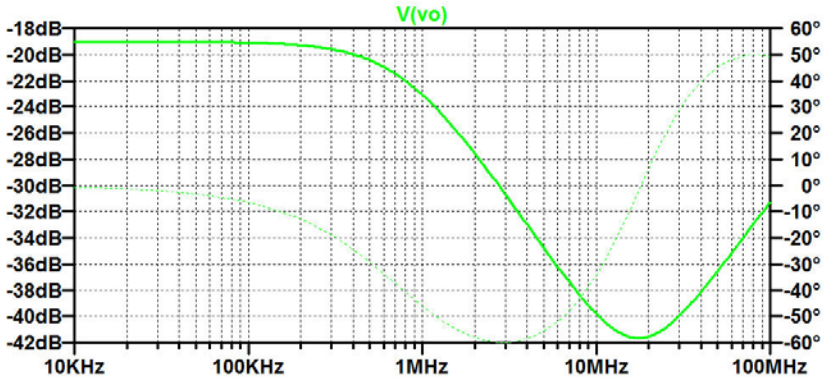
For finding the differential gain, we specify a dc value of −4.2 mV for `V1` and an ac amplitude of 0.5 V for both `V1` and `V2` in the schematic on the previous page. We use a '.ac' simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: '`.ac oct 10 10k 100Meg`'. This results in the output plot below where we find the differential low-frequency gain to be 37.6 dB and the gain-bandwidth product to be 60.7 MHz.



For finding the common-mode gain, we specify a dc value of −4.2 mV for `V1` and an ac amplitude of 0 V for both `V1` and `V2` in the schematic on the previous page. Also, we specify an ac amplitude of 1 V for `VCM`. We use a '.ac' simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: '`.ac oct 10 10k 100Meg`'. This results in the output plot below where we find the common-mode low-frequency gain to be −28.8 dB, so the common-mode rejection ratio is CMRR = 37.6 dB + 28.8 dB = 66.4 dB.



For finding the power supply rejection, we specify a dc value of −4.2 mV for `V1` and an ac amplitude of 0 V for both `V1`, `V2` and `VCM`. Also, we specify an ac amplitude of 1 V for `VDD`. We use a '.ac' simulation with a start frequency of 10 kHz and a stop frequency of 100 MHz: '`.ac oct 10 10k 100Meg`'. This results in the output plot below where we find the power supply rejection at low frequency to be 19.0 dB, so the power supply rejection ratio is PSRR = 37.6 dB + 19.0 dB = 56.6 dB



4.8

.MODEL PMOS-SH pmos (Kp=55u Vto=-0.71
+Lambda=0.16 Gamma=0.75 Phi=0.7 TOX=8n
+CGSO=0.21n CGBO=1p CGDO=0.21n CJ=1.5m
+CJSW=0.4n KF=5e-26)

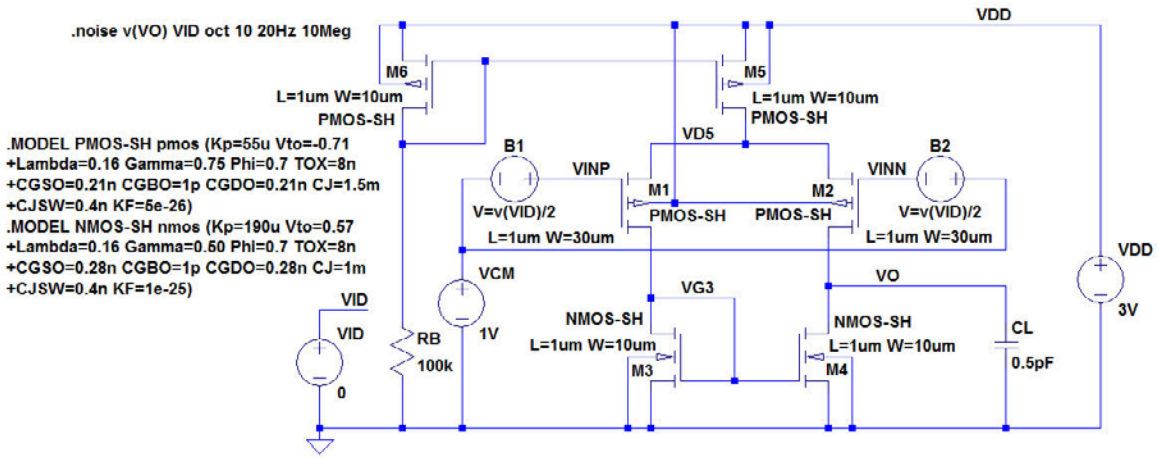
.MODEL NMOS-SH nmos (Kp=190u Vto=0.57
+Lambda=0.16 Gamma=0.50 Phi=0.7 TOX=8n
+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m
+CJSW=0.4n KF=1e-25)

Figure P4.8

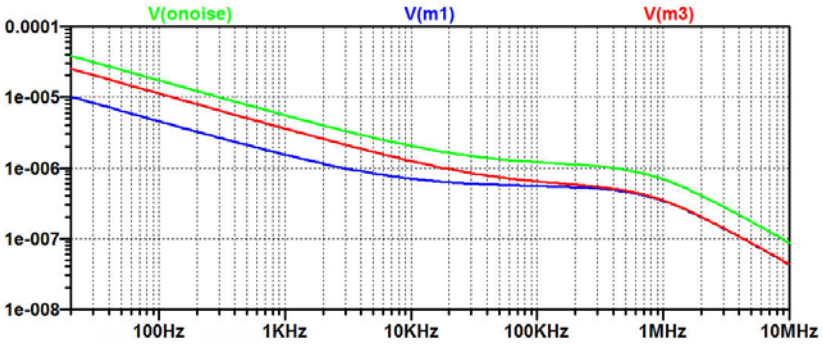
For the differential pair shown in fig. P4.7 with $W_1 = W_2 = 30$ µm, assume the transistor models shown in fig. P4.8 which include parameters for the flicker noise modelling. Plot the total noise spectral density of the output voltage and the noise contributions from M_1 and M_3 in the frequency range 20 kHz to 10 MHz, using logarithmic axes. Find the total rms output noise voltage in this frequency range. Also plot the input referred noise spectral density and find the total rms input referred noise voltage in this frequency range.

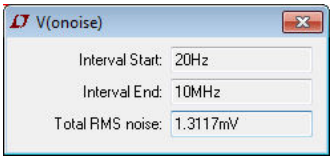
Solution:

The figure below shows the schematic in LTspice. For finding the noise voltage, we use a '.noise' simulation with `VID` as the input and `v(VO)` as the output.

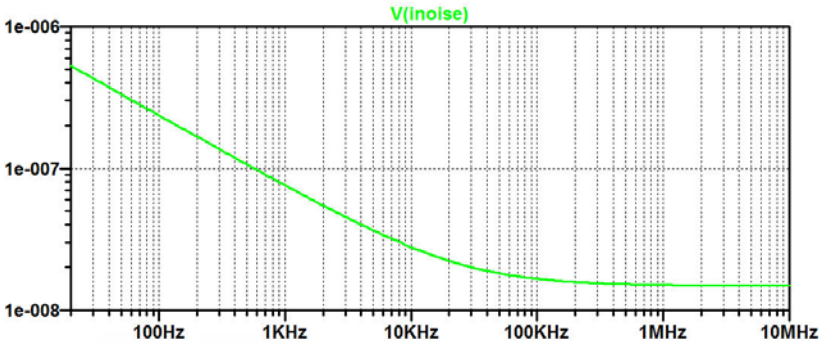


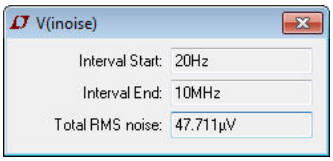
When plotting the noise contribution, remember to change the y-axis to logarithmic scale and use reasonable top and bottom limits. The output voltage is selected by pointing to the output node. The noise contributions from transistors M_1 and M_3 are selected by pointing to the transistors. The total output noise voltage is found by pointing to the green label '`V(onoise)`' above the plot and using a 'Ctrl-left click'. This opens the information window shown below, and we find $V_{on\,(\mathrm{rms})} = 1.3$ mV.





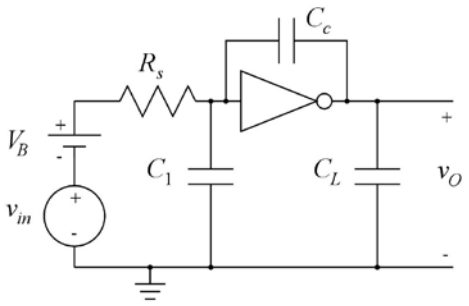
The input referred spectral noise density is selected in the plot window by the command 'Plot Settings → Visible Traces' and is shown below together with the information window resulting from a 'Ctrl-left click' on the label above the plot. We find a total equivalent input noise of $V_{in\,(\mathrm{rms})} = 48$ μV.





Tutorial 5 – Hierarchical Design

5.1



$R_s = 1$ MΩ, $V_{DD} = 3$ V,

$C_1 = 0.2$ pF, $C_c = 0.7$ pF, $C_L = 1.5$ pF.

Figure P5.1

An inverter as shown in fig. 5.25 on page 170 may be used as an inverting amplifier. Design a test bench as shown in fig. P5.1 using a supply voltage of 3 V, a minimum length of `Lmin=0.35u`, a fanout of `Fanout=1` and the BSIM3 transistor model from fig. 3.10 on page 77. Find a bias input voltage V_B which gives a bias output voltage of 1.5 V. With this value of V_B, simulate the ac response and find the dominant pole. Also, use the Miller approximation (Chan Carusone, Johns & Martin 2012) to calculate the dominant pole and compare to the simulated value.

For convenience, figs. 5.25 and 3.10 are shown below.

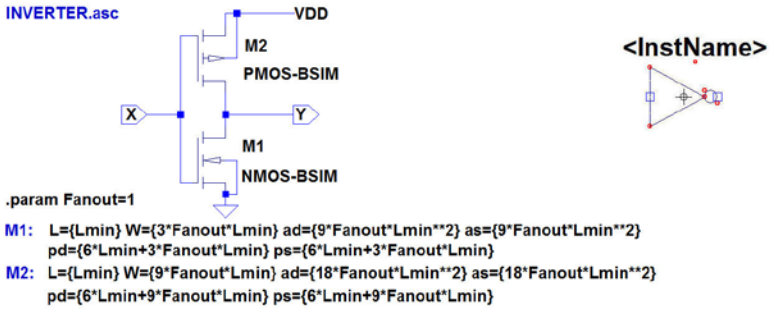


Figure 5.25: Inverter, schematic and symbol.

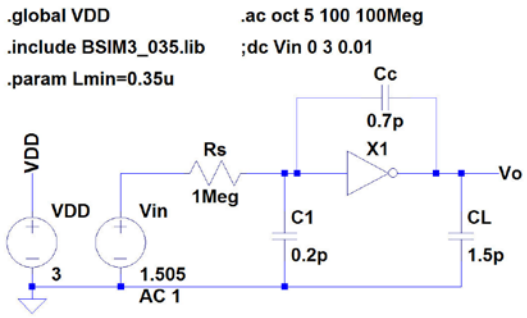
Generic BSIM3 model for 0.35 µm CMOS process. Adapted from (Chan Carusone, Johns & Martin 2014).

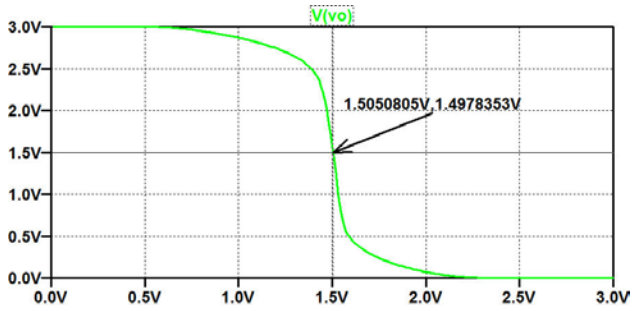
```
*BSIM3_035.lib
.MODEL NMOS-BSIM NMOS LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 7.8E-9
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = 0.48
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = 360 UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = 9e-4 PB = 7.95E-01 MJ = 3.53E-01
+CJSW = 2.8e-10 PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03

.MODEL PMOS-BSIM PMOS LEVEL = 49
+VERSION = 3.1 TNOM = 2.69E+01 TOX = 7.8E-9
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = -0.6
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = 150 UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = 14e-4 PB = 9.83E-01 MJ = 5.79E-01
+CJSW = 3.2e-10 PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure 3.10: Library file with BSIM3 models for a generic 0.35 µm CMOS process, adapted from (Chan Carusone, Johns & Martin 2014).

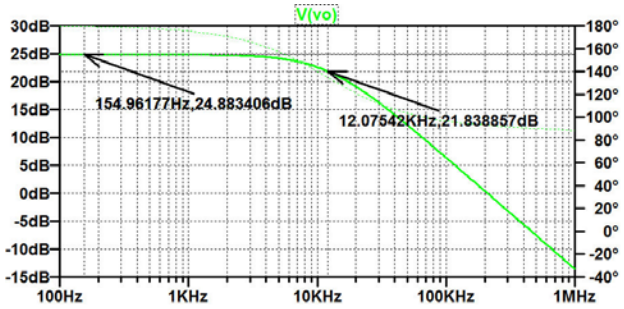
Solution:

The figure below shows the schematic drawn in LTspice. For finding the bias input voltage, we run a '.dc' simulation, the result of which is also shown below. From this, we find that a bias voltage of $V_B = 1.505$ V results in an output voltage of 1.5 V.





With 1.505 V inserted as the dc value for `Vin`, we run a '.ac' simulation from which we find a low-frequency gain of 24.9 dB (or $A_v = -17.6$ V/V) and a dominant pole of 12 kHz, see simulation plot below.



A calculation of the dominant gives $f_p = (2\pi R_s((1-A_v)C_c + C_1))^{-1} = 12$ kHz.

5.2

$$A_v(s) = \frac{\omega_{ta}(1 - s/\omega_z)}{s(1 + s/\omega_{p2})}$$

$\omega_{ta} = 2\pi \cdot 120$ MHz,
$\omega_z = 2\pi \cdot 200$ MHz,
$\omega_{p2} = 2\pi \cdot 76$ MHz.

Figure P5.2

Simulate the ac response of the closed-loop gain and the loop gain for the opamp shown in figs. 5.10 and 5.11 with $C_1 = 1$ pF, $C_2 = 0.2$ pF and $C_L = 1.5$ pF using the generic filter blocks from Table 5.3. Assume a transfer function for the opamp as specified in fig. P5.2.
Find the phase margin and the closed-loop bandwidth and compare to the results found in Example 5.2

For convenience, figs. 5.10, 5.11 and Table 5.3 are shown on the next page.

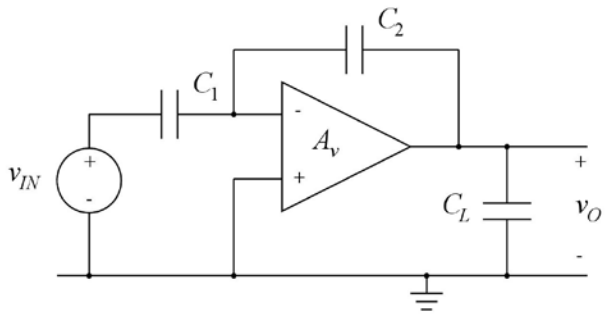


Figure 5.10: Inverting opamp configuration with capacitive feedback.

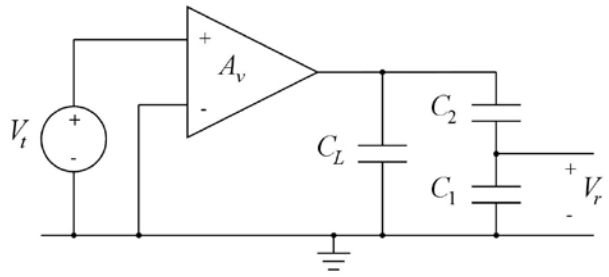


Figure 5.11: Open loop circuit for finding the loop gain $L(s) = V_r(s)/V_t(s)$.

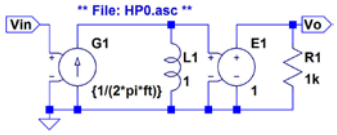
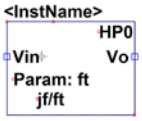
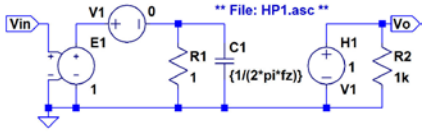
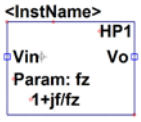
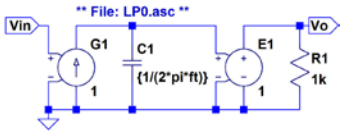
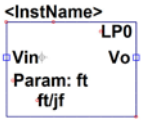
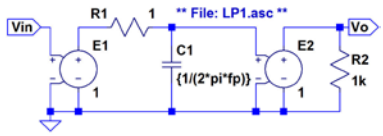
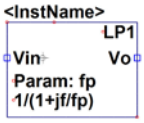
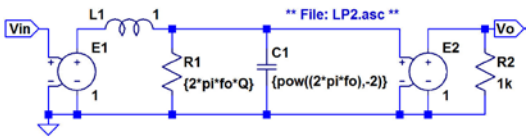
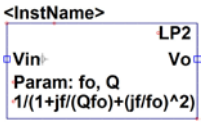
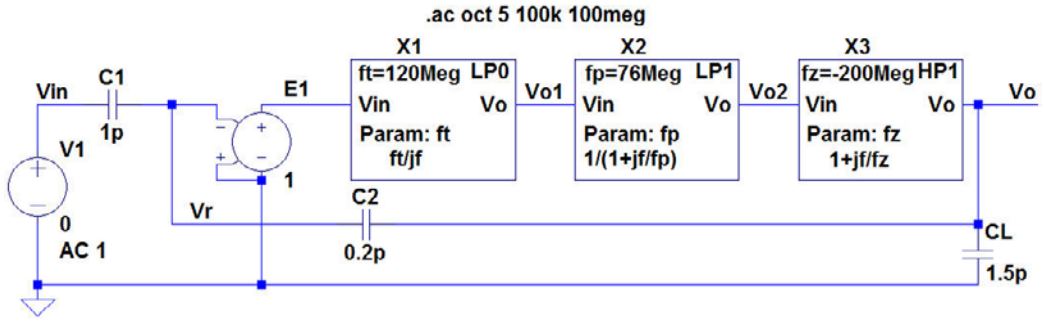
Transfer function	**Schematic**	**Symbol**	**Parameter**
Zero in 0 $T(jf) = jf/f_t$			Unity-gain frequency f_t
Real zero $T(jf) =$ $1 + jf/f_z$			Zero frequency f_z
Pole in 0 $T(jf) = f_t/(jf)$			Unity-gain frequency f_t
Real pole $T(jf) =$ $\frac{1}{1+jf/f_p}$			Pole frequency f_p
Biquad $T(jf) =$ $\frac{1}{(jf)^2+(jf)f_0/Q+f_0^2}$			Resonance frequency f_0 and quality factor Q

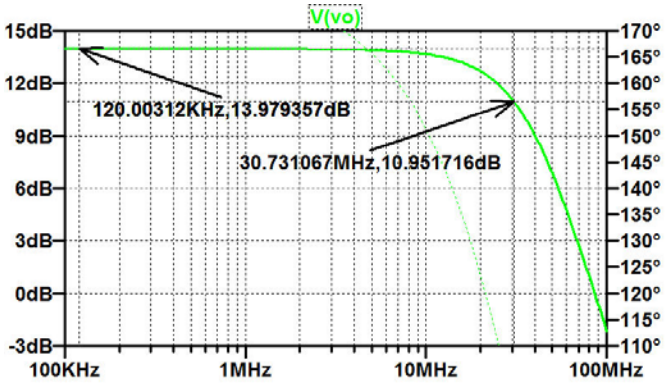
Table 5.3: Generic filter blocks defined as subcircuits.

Solution:

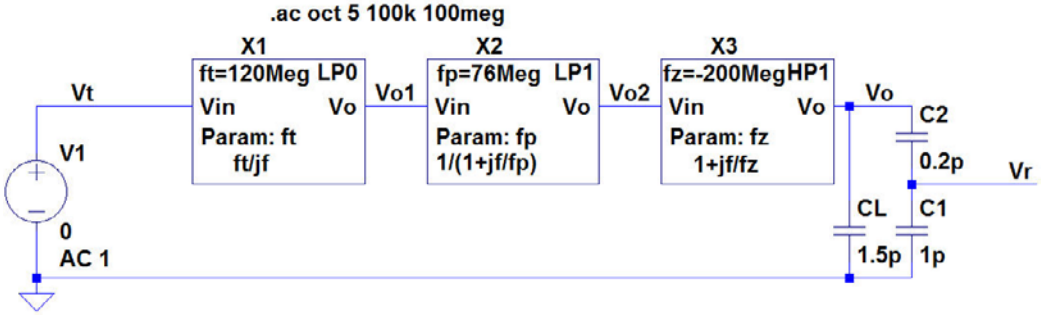
The opamp transfer function consists of a factor with a pole in 0, a factor with a real pole and a factor with a real zero. The corresponding filter blocks from Table 5.3 in 'CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide' are `LP0`, `LP1` and `HP1`.
The figure below shows the LTspice schematic corresponding to fig. 5.10 with these filter blocks inserted for the opamp and with parameters as specified in fig. P5.2. Note that the filter block `HP1` has a right half plane zero, so the parameter `fz` must be specified as a negative frequency. In order to provide an inverting input for the opamp, an inversion is obtained from the voltage controlled voltage source `E1`.

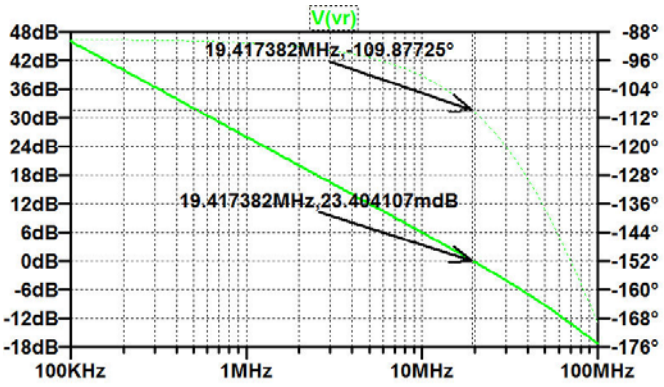


For finding the closed-loop ac response, we run a '.ac' simulation and the result of this is shown below. From the plot, we find a closed-loop bandwidth of 30.7 MHz. This is higher than the bandwidth found in Example 5.2 because higher order poles and zeros are neglected when using the opamp transfer function specified in fig. P5.2.



The figure on the next page shows the LTspice schematic corresponding to fig. 5.11.
For finding the loop gain ac response, we run a '.ac' simulation, and the result of this is also shown on the next page. From the plot, we find a phase margin of $180.0^\circ - 109.9^\circ = 70.1^\circ$. This is more than the phase margin found in Example 5.2 because higher order poles and zeros are neglected when using the opamp transfer function specified in fig. P5.2.





5.3

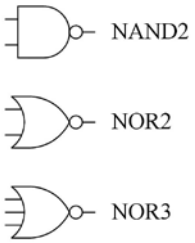


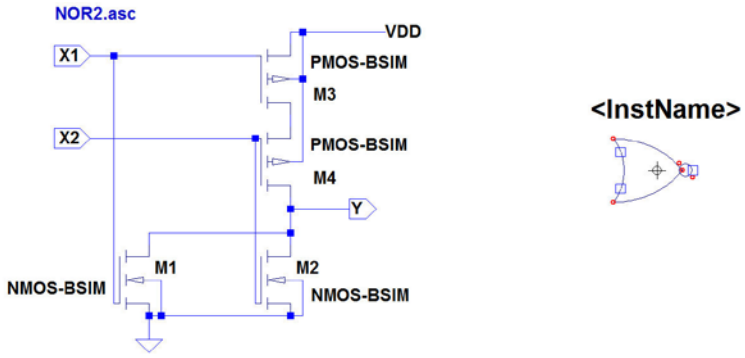
Figure P5.3

Design subcircuits for a two-input NAND gate and two-input and three-input NOR gates similar to the logic gate and inverter designs shown in Example 5.4. Scale the PMOS transistors relative to the NMOS transistors to compensate for the difference in electron mobility and hole mobility, assuming $\mu_n = 3\,\mu_p$. Use the BSIM3 transistor models from fig. 3.10 on page 77 with a channel length of $L_{min} = 0.35$ µm and a minimum channel width of $3\,L_{min}$ for NMOS transistors and $9\,L_{min}$ for PMOS transistors. What are the transistor channel widths used for the gates?

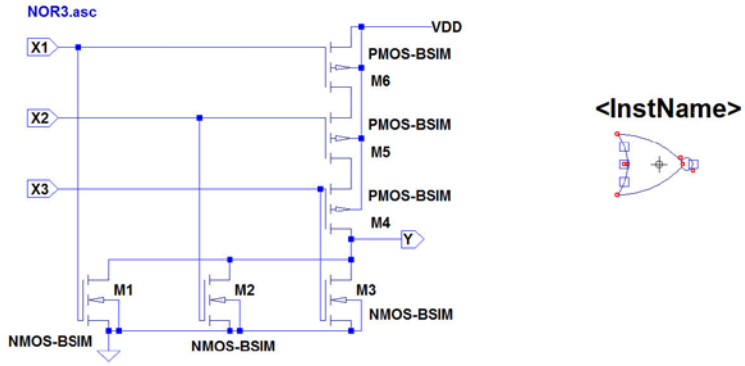
For convenience, fig. 3.10 is shown on page 72 in this book.

Solution:

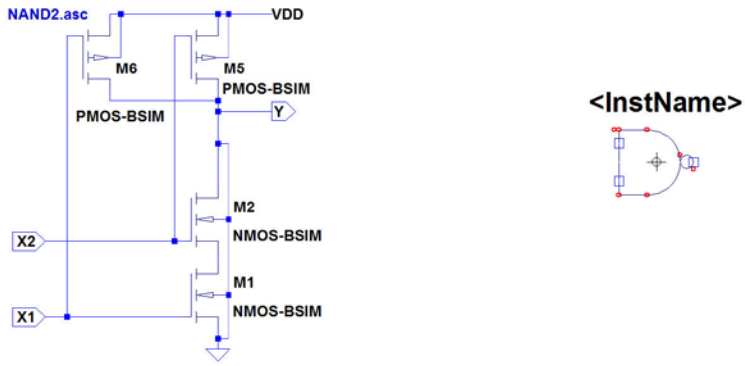
The figures below show the schematics and symbols for each of the gates NOR2, NOR3 and NAND2. In order to compensate for the difference in hole mobility and electron mobility, the channel widths have been selected as follows:
NOR2: $W_n = 3L_{min}, W_p = 18L_{min}$; NOR3: $W_n = 3L_{min}, W_p = 27L_{min}$; NAND2: $W_n = 6L_{min}, W_p = 9L_{min}$.



NMOS: NMOS-BSIM L=Lmin W={3*Lmin} ad={9*Lmin**2} as={9*Lmin**2} pd={6*Lmin} ps={6*Lmin}
PMOS: PMOS-BSIM L=Lmin W={18*Lmin} ad={54*Lmin**2} as={54*Lmin**2} pd={24*Lmin} ps={24*Lmin}



NMOS: NMOS-BSIM L=Lmin W={3*Lmin} ad={9*Lmin**2} as={9*Lmin**2} pd={6*Lmin} ps={6*Lmin}
PMOS: PMOS-BSIM L=Lmin W={27*Lmin} ad={81*Lmin**2} as={81*Lmin**2} pd={33*Lmin} ps={33*Lmin}



NMOS: NMOS-BSIM L=Lmin W={6*Lmin} ad={18*Lmin**2} as={18*Lmin**2} pd={12*Lmin} ps={12*Lmin}
PMOS: PMOS-BSIM L=Lmin W={9*Lmin} ad={27*Lmin**2} as={27*Lmin**2} pd={15*Lmin} ps={15*Lmin}

5.4

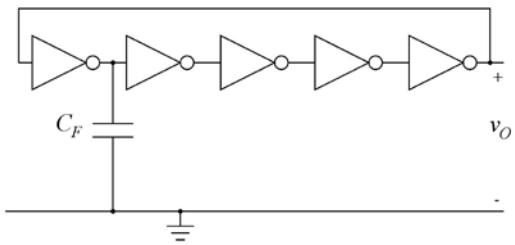


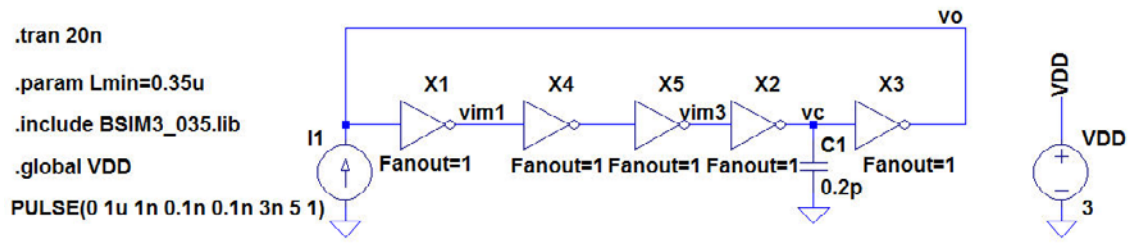
Figure P5.4

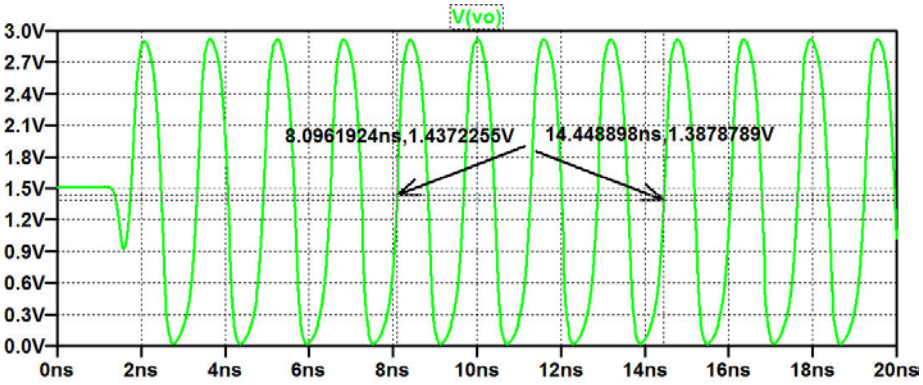
Use the inverter from fig. 5.25 on page 170 to design a ring oscillator as shown in fig. P5.4. Use the BSIM3 transistor models from fig. 3.10 on page 77 with a channel length of $L_{min} = 0.35$ µm and a supply voltage of 3 V. With `Fanout=1` and $C_F = 0.2$ pF, find the frequency of oscillation. Also find the inverter delay for an inverter loaded with an identical inverter.
Repeat for `Fanout=5` for all of the inverters.
Hint: To start the oscillation, inject a short current pulse in the output node.

For convenience, figs. 5.25 and 3.10 are shown on page 72 in this book.

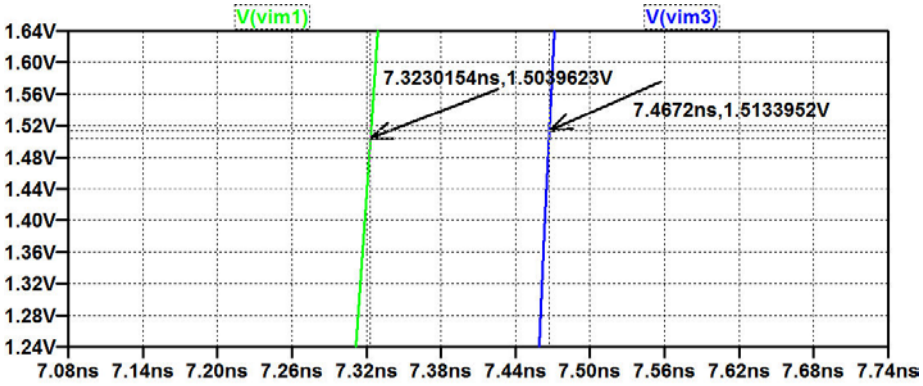
Solution:

The figure below shows the oscillator schematic in LTspice. For finding the frequency of oscillation, we run a '.tran' simulation. The resulting plot of the output voltage is shown below. Using the cursors, the time for 4 periods of oscillation, $4T$, is found, and the frequency is found as $f_{osc} = 1/T = 4/4T = 4/(14.45\text{ ns} - 8.09\text{ ns}) = 629$ MHz.





For finding the inverter delay, we plot the voltages `vim1` and `vim3` defined in the schematic. The delay between rising edges of `vim1` and `vim3` corresponds to two inverter delays. The figure below shows the simulation plot zoomed in on a short interval around 7.4 ns. Using the cursors, we find the delay from `vim1` to `vim3` to be 144 ps, so the inverter delay is 72 ps.



Repeating the simulation with a fanout of 5 for the inverters, we find $f_{osc} = 1076$ MHz and $t_{delay} = 64$ ps.

Tutorial 6 – Process and Parameter Variations

6.1

Typical model:

```
Kp=190u, Vto=0.57, Lambda=0.16
Gamma=0.5, Phi=0.7
```

Slow model:

```
Kp=170u, Vto=0.65, Lambda=0.17
Gamma=0.5, Phi=0.7
```

Fast model:

```
Kp=220u, Vto=0.45, Lambda=0.14
Gamma=0.5, Phi=0.7
```

Figure P6.1

For an NMOS transistor, assume that typical, slow and fast models are given by the Shichman-Hodges model parameters shown in fig. P6.1. Design a transistor model which combines the three models into one, using a speed parameter 'SN' with SN= −1 for the slow model, 0 for the typical model and 1 for the fast model. Find the gate-source voltage, the transconductance and the output conductance for a transistor with $V_{GS} = V_{DS}$, $I_D = 0.4$ mA, $W = 20$ µm and $L = 1$ µm for typical model parameters and for slow and fast process corners.

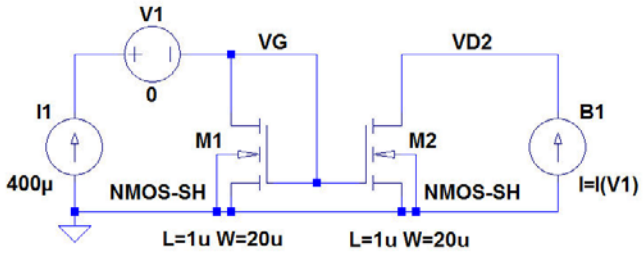
Solution:

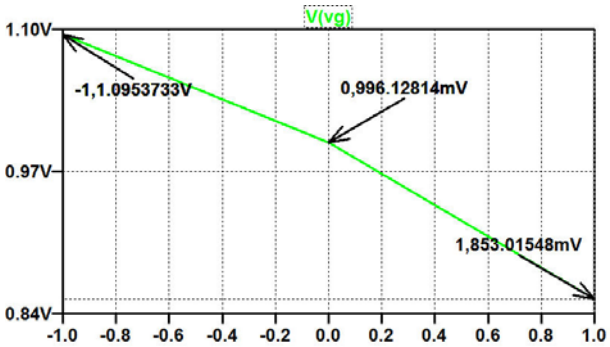
For the transistor model, we use the basic Shichman-Hodges model with `Kp`, `Vto` and `Lambda` defined as parameters. The definitions of `Kp`, `Vto` and `Lambda` are done using equation (6.4) from 'CMOS Integrated Circuit Simulation with LTspiceIV – a Tutorial Guide':

$$\texttt{X=\{Xt*(1-abs(S))+Xs*uramp(-S)+Xf*uramp(S)\}} \tag{6.4}$$

where the values for `Xt`, `Xs` and `Xf` are typical, slow and fast parameters, respectively, and `S` is the speed parameter (`SN` for an NMOS transistor and `SP` for a PMOS transistor).
The resulting model and parameter definitions are shown in the figure below.
The figure also shows a schematic for simulating V_{GS}, g_{ds} and $g_m + g_{ds}$ using the method described in Example 3.6 (fig. 3.26).
Running a '.op' simulation results in a plot window where V_{GS} can be shown versus the speed parameter `SN`. From the plot, we find: $V_{GS} = 0.996$ V for a typical transistor (`SN` = 0), $V_{GS} = 1.095$ V for a slow transistor (`SN` = -1), and $V_{GS} = 0.853$ V for a fast transistor (`SN` = 1).

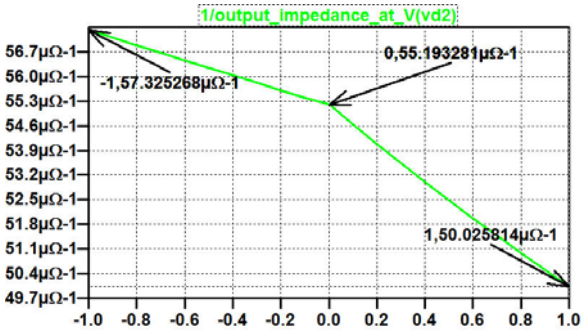
```
.model NMOS-SH NMOS (Kp={Kp} Vto={Vto} Lambda={Lambda} Gamma=0.5 Phi=0.7)
.param Kp={190u*(1-abs(SN))+170u*uramp(-SN)+220u*uramp(SN)}
.param Vto={0.57*(1-abs(SN))+0.65*uramp(-SN)+0.45*uramp(SN)}
.param Lambda={0.16*(1-abs(SN))+0.17*uramp(-SN)+0.14*uramp(SN)}
.step param SN -1 1-1

.op

;tf v(VD2) I1
```

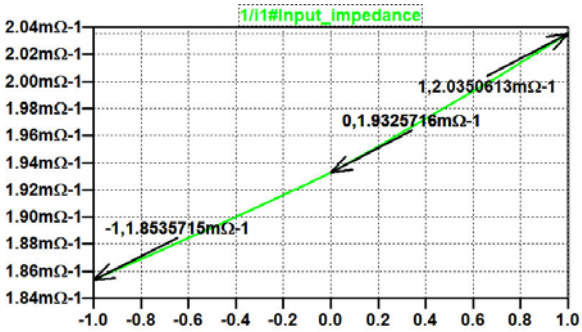




For finding the small-signal parameters, we run a '.tf' simulation (shown as a comment in the figure on the previous page).
For g_{ds}, we plot '`1/output_impedance_at_V(vd2)`'. This output conductance is equal to g_{ds} and we find: $g_{ds} = 55.2$ µA/V for a typical transistor (SN = 0), $g_{ds} = 57.3$ µA/V for a slow transistor (SN = −1), and $g_{ds} = 50.0$ µA/V for a fast transistor (SN = 1).

For finding g_m, we plot '`1/i1#input_impedance`'. This conductance is equal to $g_m + g_{ds}$, so subtracting the results for g_{ds} from the readings from the plot, we find $g_m = 1.88$ mA/V for a typical transistor (SN = 0), $g_m = 1.80$ mA/V for a slow transistor (SN = −1), and $g_m = 1.99$ mA/V for a fast transistor (SN = 1).





6.2

```
.MODEL PMOS-BSIM PMOS LEVEL = 49
*Speed parameter SP
+VERSION = 3.1 TNOM = 2.69E+01 TOX = {7.8E-9/(1+SP/20)}
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = {-0.6+SP/10}
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = {150*(1+SP/20)**2} UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = {14e-4/(1+SP/20)} PB = 9.83E-01 MJ = 5.79E-01
+CJSW = {3.2e-10/(1+SP/20)} PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure P6.2

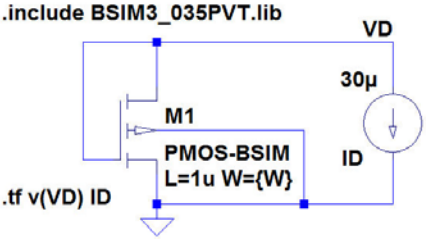
Design a PMOS transistor to provide a g_m of at least 0.48 mA/V with $V_{GS} = V_{DS}$ and $I_D = 30$ µA using a worst-case combination of temperature and process variations. Assume the BSIM3 model shown in fig. P6.2 and a temperature range from -40°C to 85°C. Use a channel length of $L = 1$ µm.

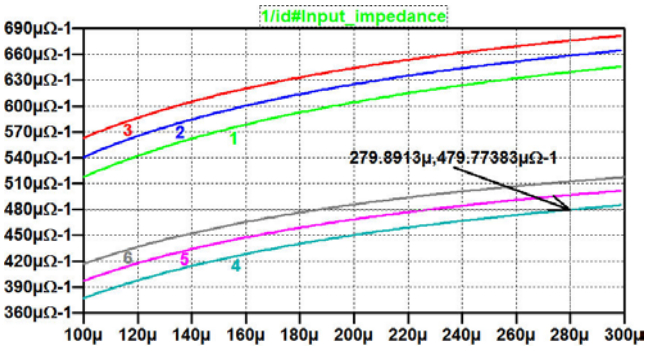
Solution:

For finding g_m versus the channel width W, we use the approach shown in fig. 6.5. The schematic from fig. 6.5 is shown on the next page for a PMOS transistor. For a transistor with $L = 1$ µm, we assume $g_m \gg g_{ds}$, so the small-signal resistance of the diode-connected transistor is a good approximation to $1/g_m$.

For showing both temperature variations and process parameter variations, we step both temperature and speed parameter as shown in the schematic on the next page. The '.step' directives are inserted with the W-command first, so that the x-axis of the plot is W. Next, the SP-command is inserted and finally the '.temp' command. Then the three curves for a temperature of -40°C are runs 1 to 3 (starting with SP = -1), and the three curves for a temperature of 85°C are runs 4 to 6 (starting with SP = -1). From the plot of '1/i1#input_impedance', we find that the worst-case corner is a slow transistor operating at 85°C, and we find that $W = 280$ µm is required to obtain $g_m \geq 0.48$ mA/V.

```
.step param W 100u 300u 5u
.step param sp -1 1 1
.temp -40 85
.include BSIM3_035PVT.lib
```





6.3

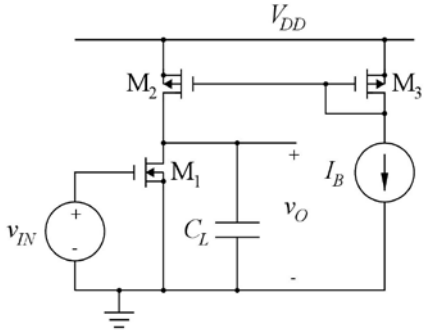


Figure P6.3

For the common-source stage shown in fig. P6.3, assume $L_1 = L_2 = L_3 = 1$ μm, $W_1 = 22$ μm, $W_2 = W_3 = 20$ μm, $I_B = 140$ μA and $V_{DD} = 3$ V. Assume the BSIM3 models shown in fig. 6.2 on page 184 and a temperature of 27°C. Also assume that process variations cause C_L to have a value in the range of 1.3 pF to 1.7 pF. Find the process corners for the unity-gain frequency.

For convenience, fig. 6.2 is shown below.

Generic BSIM3 model for 0.35 μm CMOS process with speed parameters SN and SP to define process variations.

```
*BSIM3_035PVT.lib
.MODEL NMOS-BSIM NMOS LEVEL = 49
*Speed parameter SN
+VERSION = 3.1 TNOM = 27 TOX = {7.8E-9/(1+SN/20)}
+XJ = 1E-07 NCH = 2.18E+17 VTH0 = {0.48-SN/10}
+K1 = 6.07E-01 K2 = 1.24E-03 K3 = 9.68E+01
+K3B = -9.84E+00 W0 = 2.02E-05 NLX = 1.62E-07
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.87E+00 DVT1 = 5.86E-01 DVT2 = -1.26E-01
+U0 = {360*(1+SN/20)**2} UA = -8.48E-10 UB = 2.27E-18
+UC = 3.27E-11 VSAT = 1.87E+05 A0 = 1.22E+00
+AGS = 2.06E-01 B0 = 9.60E-07 B1 = 4.95E-06
+KETA = -1.67E-04 A1 = 0 A2 = 3.49E-01
+RDSW = 8.18E+02 PRWG = 2.35E-02 PRWB = -8.12E-02
+WR = 9.98E-01 WINT = 1.55E-07 LINT = 4.51E-10
+DWG = -4.27E-09
+DWB = 4.07E-09 VOFF = -4.14E-02 NFACTOR = 1.61E+00
+CIT = 0 CDSC = 2.39E-04 CDSCD = 0.00E+00
+CDSCB = 0 ETA0 = 1 ETAB = -1.99E-01
+DSUB = 1 PCLM = 1.32E+00 PDIBLC1 = 2.42E-04
+PDIBLC2 = 8.27E-03 PDIBLCB = -9.99E-04 DROUT = 9.72E-04
+PSCBE1 = 7.24E+08 PSCBE2 = 9.96E-04 PVAG = 1.00E-02
+DELTA = 1.01E-02 RSH = 3.33E+00 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.11E-01
+KT1L = 0 KT2 = 2.22E-02 UA1 = 4.34E-09
+UB1 = -7.56E-18 UC1 = -5.62E-11 AT = 3.31E+04
+WL = 0 WLN = 9.95E-01 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.76E-10 CGSO = 2.76E-10 CGBO = 1.00E-12
+CJ = {9e-4/(1+SN/20)} PB = 7.95E-01 MJ = 3.53E-01
+CJSW = {2.8e-10/(1+SN/20)} PBSW = 7.98E-01 MJSW = 1.73E-01
+CJSWG = 1.81E-10 PBSWG = 7.96E-01 MJSWG = 1.74E-01
+CF = 0 PVTH0 = -1.80E-02 PRDSW = -7.56E+01
+PK2 = 4.48E-05 WKETA = -1.33E-03 LKETA = -8.91E-03

.MODEL PMOS-BSIM PMOS LEVEL = 49
*Speed parameter SP
+VERSION = 3.1 TNOM = 2.69E+01 TOX = {7.8E-9/(1+SP/20)}
+XJ = 1.00E-07 NCH = 8.44E+16 VTH0 = {-0.6+SP/10}
+K1 = 4.82E-01 K2 = -2.13E-02 K3 = 8.27E+01
+K3B = -5 W0 = 5.24E-06 NLX = 2.49E-07
+DVT0W = 0.00E+00 DVT1W = 0 DVT2W = 0
+DVT0 = 3.54E-01 DVT1 = 7.52E-01 DVT2 = -2.98E-01
+U0 = {150*(1+SP/20)**2} UA = 1E-10 UB = 1.75E-18
+UC = -2.27E-11 VSAT = 2.01E+05 A0 = 1.04E+00
+AGS = 2.90E-01 B0 = 1.94E-06 B1 = 5.01E-06
+KETA = -3.85E-03 A1 = 4.20E-03 A2 = 1.00E+00
+RDSW = 4000 PRWG = -9.54E-02 PRWB = -1.92E-03
+WR = 1 WINT = 1.47E-07 LINT = 1.04E-10
+DWG = -1.09E-08
+DWB = 1.14E-08 VOFF = -1.29E-01 NFACTOR = 2.01E+00
+CIT = 0 CDSC = 2.40E-04 CDSCD = 0
+CDSCB = 0 ETA0 = 4.07E-02 ETAB = 6.84E-03
+DSUB = 3.21E-01 PCLM = 5.96E+00 PDIBLC1 = 2.89E-03
+PDIBLC2 = -1.45E-06 PDIBLCB = -1E-03 DROUT = 9.93E-04
+PSCBE1 = 7.88E+10 PSCBE2 = 5E-10 PVAG = 15
+DELTA = 9.96E-03 RSH = 2.6 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -1.09E-01
+KT1L = 0 KT2 = 2.19E-02 UA1 = 4.34E-09
+UB1 = -7.62E-18 UC1 = -5.63E-11 AT = 3.28E+04
+WL = 0 WLN = 1 WW = 0
+WWN = 1.00E+00 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2.01E+00 XPART = 0.5
+CGDO = 2.10E-10 CGSO = 2.12E-10 CGBO = 1.00E-12
+CJ = {14e-4/(1+SP/20)} PB = 9.83E-01 MJ = 5.79E-01
+CJSW = {3.2e-10/(1+SP/20)} PBSW = 9.92E-01 MJSW = 3.60E-01
+CJSWG = 4.41E-11 PBSWG = 9.85E-01 MJSWG = 3.58E-01
+CF = 0 PVTH0 = 2.58E-02 PRDSW = -3.98E+01
+PK2 = 2.02E-03 WKETA = 2.72E-03 LKETA = -7.14E-03
```

Figure 6.2: Library file with BSIM3 models for a generic 0.35 μm CMOS process with speed parameters SN and SP to define process variations, adapted from (Chan Carusone, Johns & Martin 2014). Speed parameter is 0 for typical model, –1 for slow model and +1 for fast model.

Solution:

For simulating the unity-gain frequency, we need a '.ac' simulation. In order to ensure a correct dc bias point for the '.ac' simulation in all process corners, we apply a dc feedback as shown in fig. 6.15(a). For convenience, this figure is shown below.

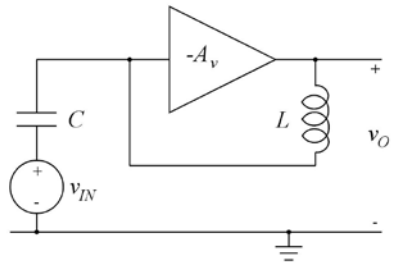
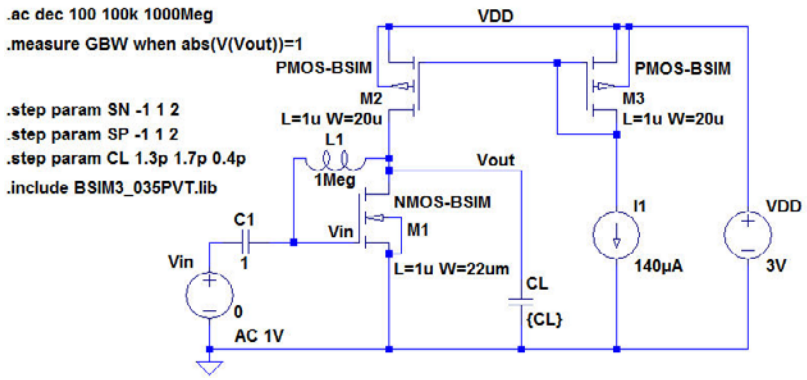
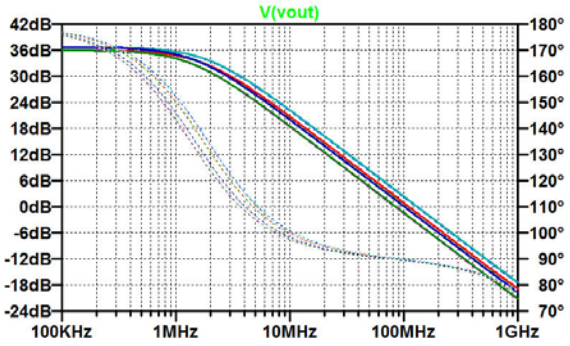


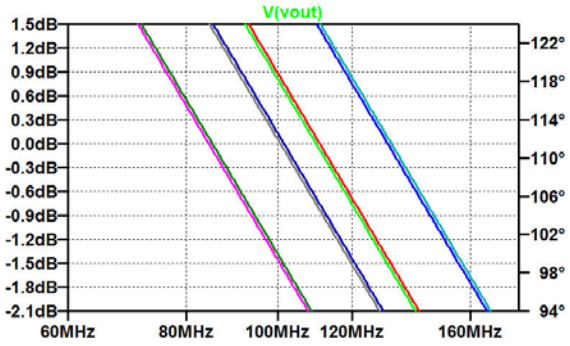
Figure 6.15(a): Inverting amplifier with dc feedback to provide a suitable dc bias point.

For finding the process corners, we step the speed parameters SN and SP between the values -1 and 1, and we step the capacitor C_L between the two values 1.3 pF (fast) and 1.7 pF (slow) using the '.step' commands shown in the schematic below. The '.step' directives are inserted with the SN-command first, so that SN is stepped first. Next, the SP-command is inserted and finally the C_L-command. We may find the unity-gain frequency from the plots resulting from a '.ac' simulation but it is easier to use a '.measure' directive as shown in the schematic below.



The plot resulting from a '.ac' simulation is shown below. It has a total of eight traces, one for each corner, but some of the traces are almost overlapping. This can be seen from the close-up on the plot around the unity-gain frequency also shown below.





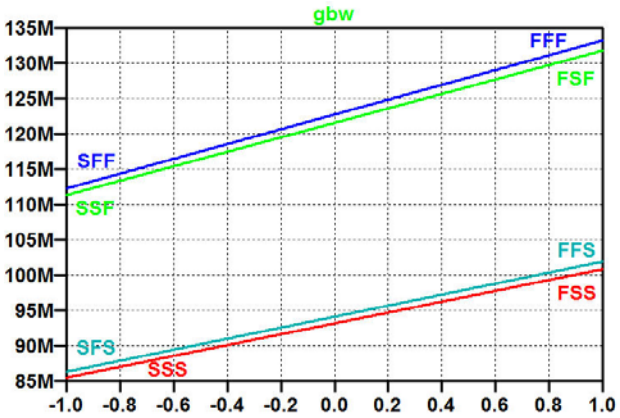
Rather than using the cursors to find the process corners, we use the results from the '.measure' directive found in the error log file ('Ctrl-L') shown below.

```
Direct Newton iteration for .op point succeeded.
.step sn=-1 sp=-1 cl=1.3e-012
.step sn=1 sp=-1 cl=1.3e-012
.step sn=-1 sp=1 cl=1.3e-012
.step sn=1 sp=1 cl=1.3e-012
.step sn=-1 sp=-1 cl=1.7e-012
.step sn=1 sp=-1 cl=1.7e-012
.step sn=-1 sp=1 cl=1.7e-012
.step sn=1 sp=1 cl=1.7e-012


Measurement: gbw
  step     abs(v(vout))=1
     1     1.11258e+008
     2     1.3178e+008
     3     1.12261e+008
     4     1.33161e+008
     5     8.54866e+007
     6     1.00804e+008
     7     8.62869e+007
     8     1.01908e+008
```

From this, we can compile the following table:

Step	NMOS	PMOS	C_L	Unity-gain frequency
1	slow	slow	fast	111.3 MHz
2	fast	slow	fast	131.8 MHz
3	slow	fast	fast	112.3 MHz
4	fast	fast	fast	133.2 MHz
5	slow	slow	slow	85.5 MHz
6	fast	slow	slow	100.8 MHz
7	slow	fast	slow	86.3 MHz
8	fast	fast	slow	101.9 MHz

The results may also be shown graphically by right clicking in the error log file and selecting 'Plot .step'ed .meas data'. The figure below shows this plot with a labelling indicating the process corners.



6.4

For the digital inverter `X2` in fig. 6.18 on page 196, find the worst-case delay time considering both process variations, temperature variations from -40°C to 85°C and supply voltage variations from 2.7 V to 3.3 V.

For convenience, fig. 6.18 is shown below.

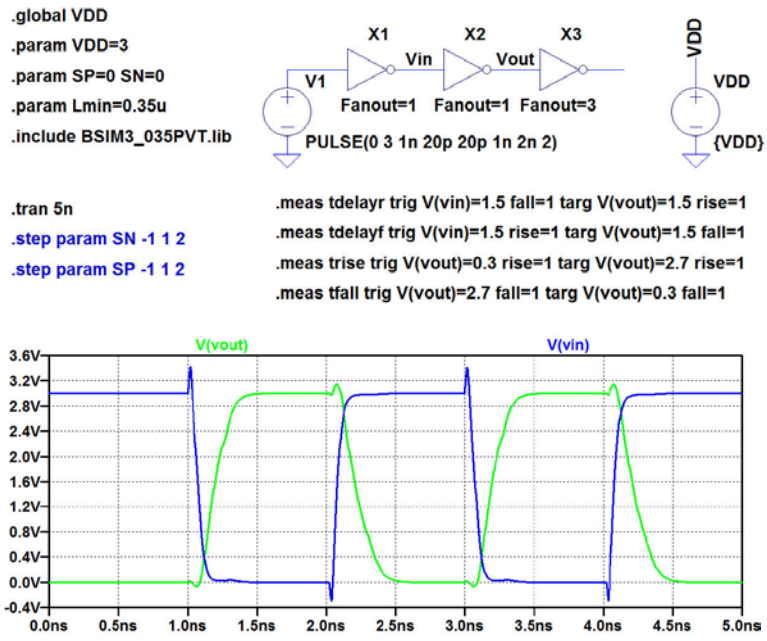


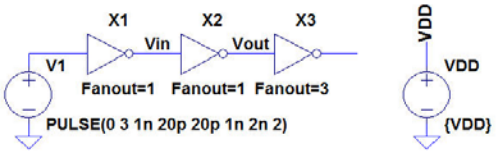
Figure 6.18: LTspice schematic of the inverter used as a digital inverter (top) and the result of a transient simulation (bottom).

Solution:

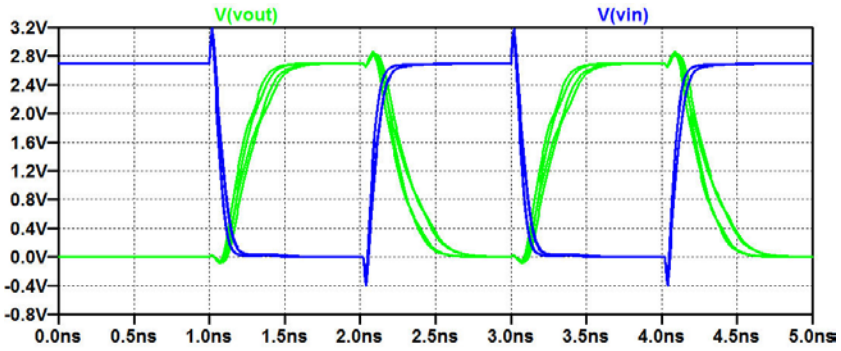
Compared to the simulation in fig. 6.18, we need to vary also the temperature and the supply voltage. Thus, we have a total of four parameters to be stepped which is more than LTspice can handle. However, we know from the simulations of the transistor characteristics that the high temperature (85°C) is the more critical one, and – intuitively – a low supply voltage will give longer delays as the transistor overdrive voltages are smaller. Thus, a pragmatic approach is to repeat the simulation from fig. 6.18 with a temperature of 85°C and a supply voltage of 2.7 V. In the '.meas' directives, the threshold voltages for rising and falling edge should be modified accordingly, i.e. to $V_{DD}/2$ V. Also the threshold voltages for rise time and fall time are modified although rise and fall time simulations are not requested in the problem.

The schematic with these changes are shown on the next page, and also a plot from the transient simulation and the results from the error log file are shown. We find that the worst-case delay occurs for a falling output with a slow NMOS transistor and a fast PMOS transistor. The maximum delay time is 199 ps. Also shown on the next page is a close-up on the falling output edge around 2 ns. The up and down arrow keys are used to place the cursor on the correct trace (step 3) and a right mouse click on the cursor is used to open a window with information about which trace the cursor is following.

```
.global VDD
.param VDD=2.7
.param SP=-1 SN=-1
.param Lmin=0.35u
.include BSIM3_035PVT.lib
.temp 85

.tran 5n
.step param SN -1 1 2
.step param SP -1 1 2
```

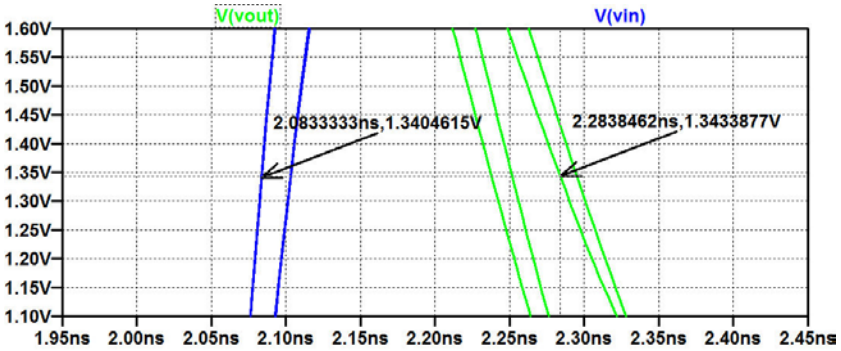


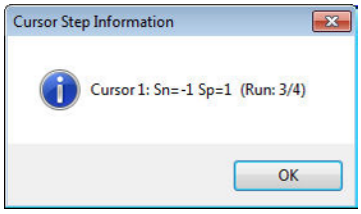

```
.meas tdelayr trig V(vin)={VDD/2} fall=1 targ V(vout)={VDD/2} rise=1
.meas tdelayf trig V(vin)={VDD/2} rise=1 targ V(vout)={VDD/2} fall=1
.meas trise trig V(vout)={VDD*0.1} rise=1 targ V(vout)={VDD*0.9} rise=1
.meas tfall trig V(vout)={VDD*0.9} fall=1 targ V(vout)={VDD*0.1} fall=1
```




```
Direct Newton iteration for .op point succeeded.
.step sn=-1 sp=-1
.step sn=1 sp=-1
.step sn=-1 sp=1
.step sn=1 sp=1
```

```
Measurement: tdelayr
  step            tdelayr            FROM               TO
     1            1.76492e-010       1.0868e-009        1.26329e-009
     2            1.75295e-010       1.06988e-009       1.24517e-009
     3            1.32493e-010       1.08991e-009       1.2224e-009
     4            1.30468e-010       1.07231e-009       1.20278e-009

Measurement: tdelayf
  step            tdelayf            FROM               TO
     1            1.90873e-010       2.1032e-009        2.29407e-009
     2            1.47291e-010       2.10361e-009       2.2509e-009
     3            1.99271e-010       2.08364e-009       2.28291e-009
     4            1.53242e-010       2.08384e-009       2.23708e-009
```





6.5

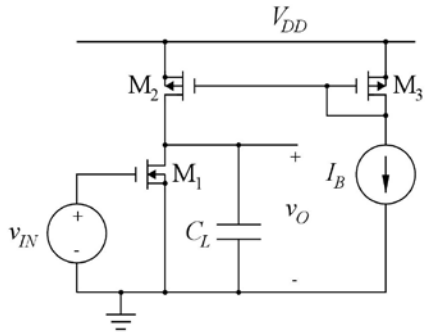
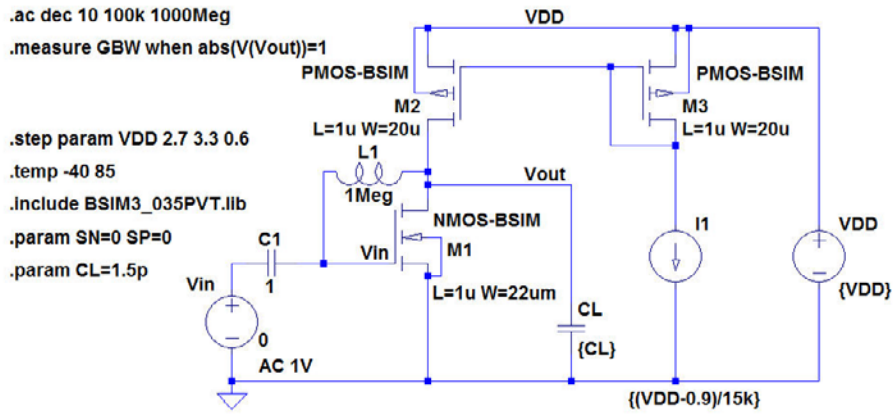


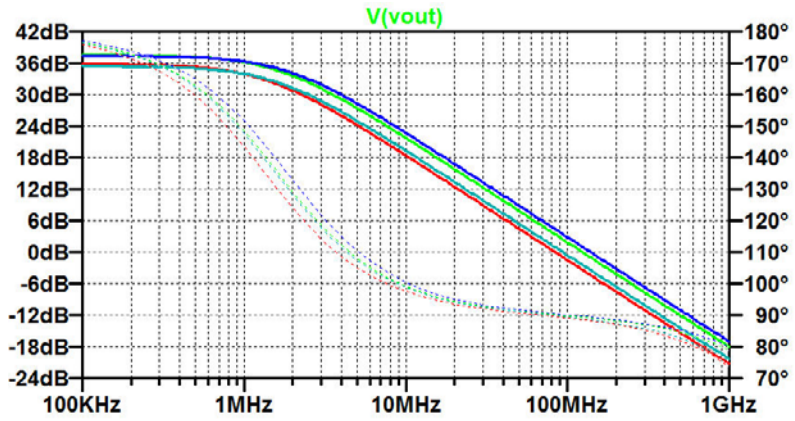
Figure P6.5

For the common-source stage shown in fig. P6.5, find the worst-case corner for unity-gain bandwidth (lowest unity-gain bandwidth) for temperature variations and supply voltage variations. Assume $C_L = 1.5$ pF, $L_1 = L_2 = L_3 = 1$ µm, $W_1 = 22$ µm, $W_2 = W_3 = 20$ µm, $I_B = (V_{DD} - 0.9\text{ V})/(15\text{ k}\Omega)$ and $V_{DD} = 3$ V. Assume the BSIM3 models shown in fig. 6.2 on page 184 with typical process parameters, temperature variations from -40°C to 85°C and supply voltage variations from 2.7 V to 3.3 V. Run a Monte Carlo simulation for the worst-case combination of temperature and supply voltage with stochastic variations of the process parameters for the transistors and the capacitor C_L. Assume a standard deviation of 0.4 for the process speed parameters and a capacitor tolerance of $\pm 5\%$. Estimate mean value and standard deviation of the unity-gain frequency for the worst-case combination of temperature and supply voltage.

Solution:

For simulating the unity-gain frequency, we need a '.ac' simulation. In order to ensure a correct dc bias point for the '.ac' simulation in all process corners, we apply a dc feedback as shown in fig. 6.15(a) (also shown on page 89 in this book). For finding corners for supply voltage variation and temperature variation, we step the supply voltage VDD and the temperature using the '.step' command and the '.temp' command shown in the schematic on the next page. We may find the unity-gain frequency from the plots resulting from a '.ac' simulation but it is easier to use a '.measure' directive to calculate the process corner values of the unity-gain frequency. The '.measure' directive is shown in the schematic on the next page.

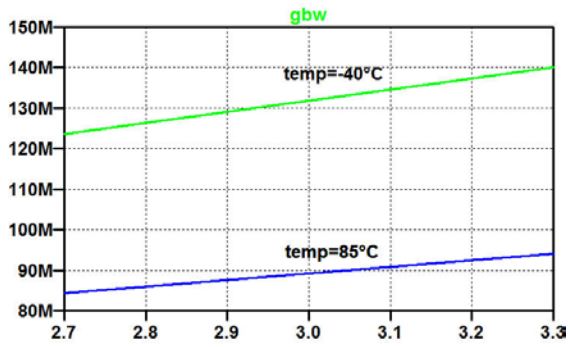




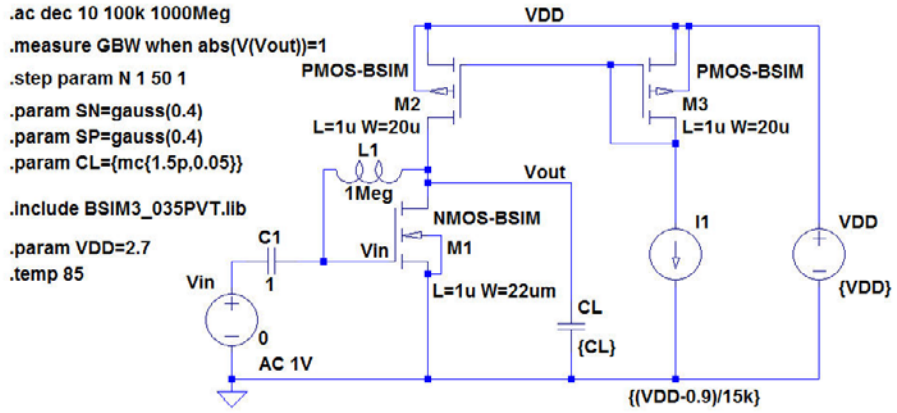
The results from the '.measure' directive are found in the error log file shown below, and we find that the worst-case corner is the combination of a low supply voltage and a high temperature.

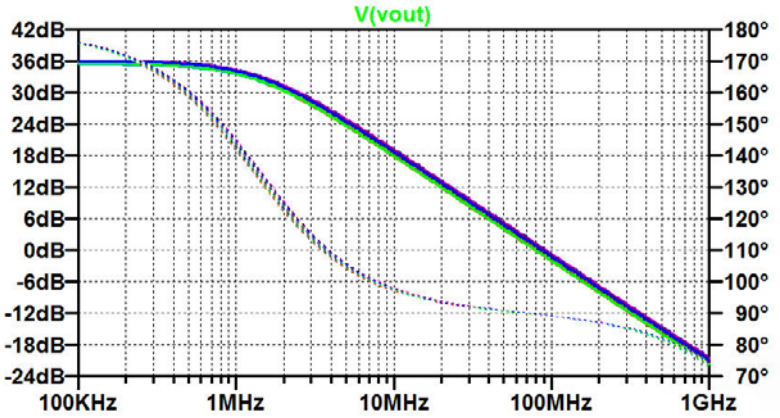
The process corners can also be shown graphically by right clicking in the error log file and selecting 'Plot .step'ed .meas data'. The figure below shows the resulting plot.

```
Direct Newton iteration for .op point succeeded.
.step vdd=2.7 temp=-40°C
.step vdd=3.3 temp=-40°C
.step vdd=2.7 temp=85°C
.step vdd=3.3 temp=85°C


Measurement: gbw
  step             abs(v(vout))=1
     1             1.23642e+008
     2             1.39998e+008
     3             8.42695e+007
     4             9.40421e+007
```



For running a Monte Carlo simulation with a supply voltage of 2.7 V and a temperature of 85°C, we define `VDD` and `temp` to have these values. Also, we define `SN`, `SP` and `CL` to have stochastic variations using the functions '`gauss(x)`' and '`mc(x,y)`'. For a Monte Carlo simulation with 50 simulations, a step count parameter `N` must be defined as shown in the schematic below. Also a plot of the output voltage resulting from the simulation is shown.

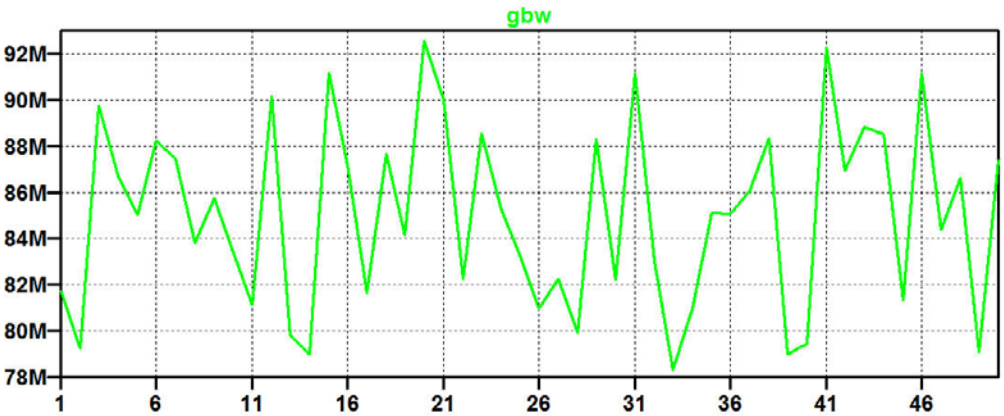




The error log file from the simulation gives the calculated values of the unity-gain bandwidth for each of the 50 steps in the Monte Carlo simulation. The results are shown on the next page. By right clicking in the error log file and selecting 'Plot .step'ed .meas data', the results can also be plotted graphically as also shown on the next page.

The results from the error log file may be copied into an Excel spreadsheet, and from this, we find a mean value of 85 MHz and a standard deviation of 4 MHz.

```
Measurement: gbw
  step             abs(v(vout))=1
     1             8.17271e+007
     2             7.92561e+007
     3             8.97408e+007
     4             8.67015e+007
     5             8.50062e+007
     6             8.82216e+007
     7             8.74819e+007
     8             8.38107e+007
     9             8.57428e+007
    10             8.34513e+007
    11             8.11149e+007
    12             9.0147e+007
    13             7.982e+007
    14             7.90185e+007
    15             9.11583e+007
    16             8.71882e+007
    17             8.1665e+007
    18             8.76643e+007
    19             8.4134e+007
    20             9.25686e+007
    21             9.00365e+007
    22             8.22461e+007
    23             8.85673e+007
    24             8.5306e+007
    25             8.32077e+007
    26             8.09493e+007
    27             8.22352e+007
    28             7.99386e+007
    29             8.83158e+007
    30             8.22246e+007
    31             9.11552e+007
    32             8.30066e+007
    33             7.83127e+007
    34             8.09654e+007
    35             8.51145e+007
    36             8.50773e+007
    37             8.60746e+007
    38             8.83669e+007
    39             7.90209e+007
    40             7.94301e+007
    41             9.22594e+007
    42             8.69342e+007
    43             8.88345e+007
    44             8.85208e+007
    45             8.13371e+007
    46             9.11521e+007
    47             8.43626e+007
    48             8.66154e+007
    49             7.90699e+007
    50             8.74e+007
```



Tutorial 7 – Importing and Exporting Files

7.1

```
*Differential NMOS pair with
*resistive load and differential output

*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground

*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u
```

Figure P7.1

Fig. 3.10 is shown on page 72 in this book.

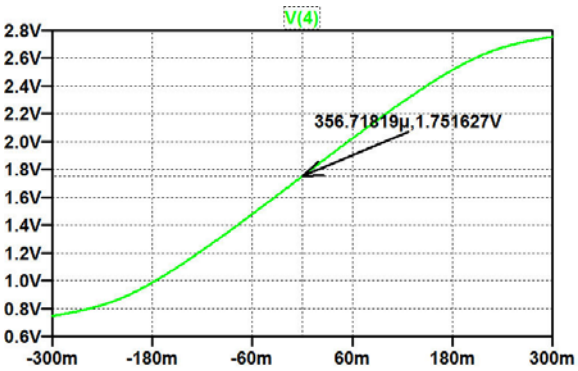
Fig. P7.1 shows a netlist for a differential NMOS pair with differential output. Create a netlist file for LTspice for simulating the circuit with a supply voltage of 3 V, a bias current of 250 μA and a common-mode input voltage of 1.5 V. Use the BSIM3 transistor model from fig. 3.10 on page 77. Find the bias values of the output voltages and the small-signal differential gain.

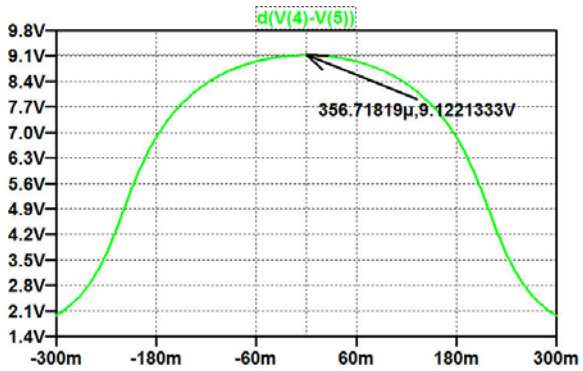
Solution:

For the netlist file for LTspice, we need to add the supply voltage, the bias current, and the input voltages (common-mode and differential-mode). Also, a simulation directive must be specified. In the file shown below, the input voltages are added using the scheme from problem 4.6, and the differential input voltage is varied using a '.step' directive in combination with a '.op' simulation.

```
*Differential NMOS pair with
*resistive load and differential output

*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground

*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u

*Transistor models

.include BSIM3_035.lib

*Supply voltage and bias current

VDD 1 0 3
IB 6 0 250u

*input voltages

vcm 11 0 1.5
vdp 3 11 {vid/2}
vdn 2 11 {-vid/2}

.step param vid -0.3 0.3 0.001

.op

.end
```

The simulation is run directly from the netlist file in LTspice using the 'Simulate → Run' command (or 'Ctrl-R'), and in the plot window which opens, the traces to plot are selected using 'Plot Setting → Add trace' (or 'Ctrl-A'). For finding the common-mode output voltage, we plot the noninverting output (`V(4)`) and read the value for an input voltage of 0 V. For finding the differential gain, we plot the derivative of the differential output voltage, i.e. `d(V(4)-V(5))` and find the value for an input voltage of 0 V. From the plots below, we find a common-mode output voltage of 1.75 V and a differential gain of 9.12 V/V.





7.2

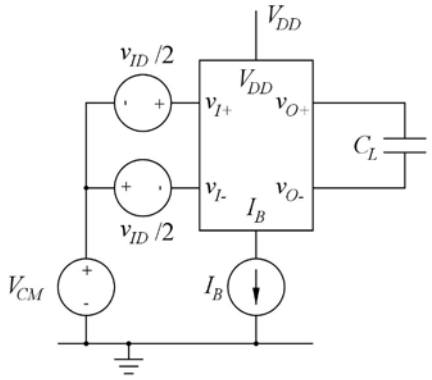


Figure P7.2

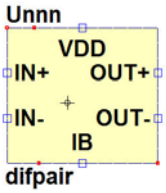
Use the netlist from fig. P7.1 to design a subcircuit and a subcircuit symbol for the differential pair. Use the BSIM3 transistor model from fig. 3.10 on page 77. Design the subcircuit to have separate terminals for the supply voltage and the bias current. Insert the differential pair in a test bench as shown in fig. P7.2 and find the -3 dB frequency for the differential gain. Use $V_{DD} = 3$ V, $I_B = 250$ µA, $V_{CM} = 1.5$ V and $C_L = 3$ pF.

Fig. 3.10 is shown on page 72 in this book.

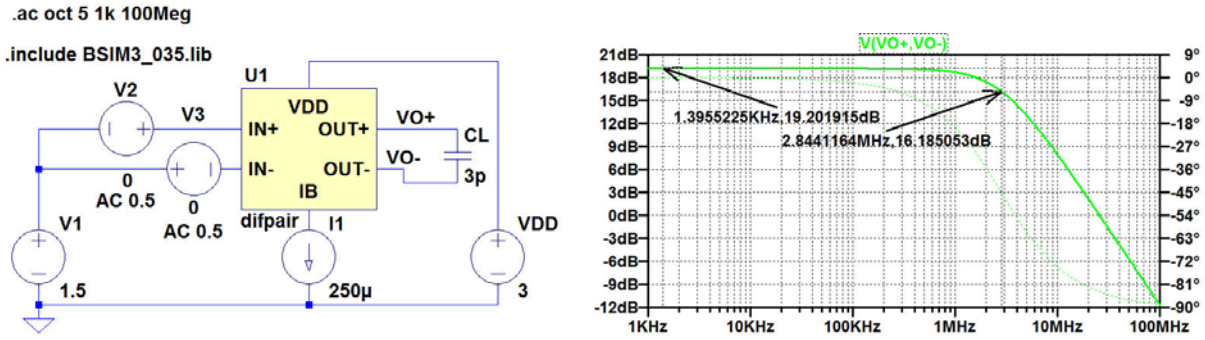
Solution:

The netlist from fig. P7.1 is modified by including a '.subckt' directive and a '.ends' directive as shown below. By placing the cursor in the '.subckt' line and right clicking, a symbol is generated, and using the graphic symbol editor, this may be modified into the symbol shown below.

```
*Differential NMOS pair with
*resistive load and differential output

*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground

.subckt difpair 1 2 3 4 5 6

*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W=16u
M2 5 3 6 0 NMOS-BSIM L=0.7u W=16u

.ends
```



The figure below shows a testbench corresponding to fig. P7.2 and a plot of the differential output voltage. From the plot, we find a −3 dB frequency of 2.84 MHz.



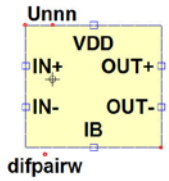
7.3

Redefine the subcircuit from problem 7.2 to have the transistor channel width as a parameter which can be defined at top level.
Use the testbench from fig. P7.2 to find the low-frequency gain as a function of the channel width for 5 µm$\leq W \leq$ 30 µm. What is the value of the low-frequency gain for $W = 5$ µm and $W =$ 30 µm?

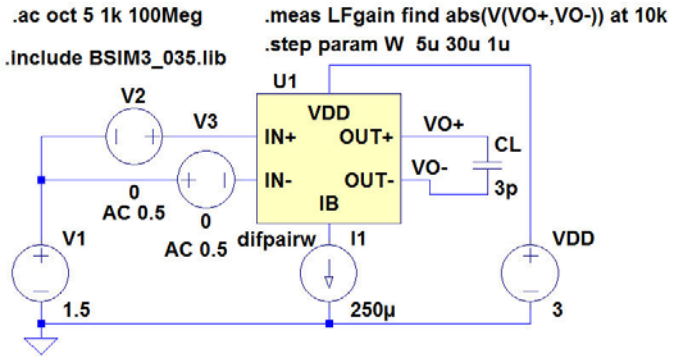
Solution:

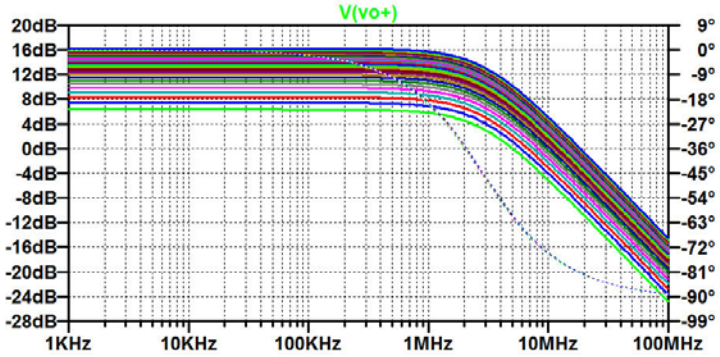
The netlist from problem 7.2 is modified by specifying the channel width as a parameter. Also, the subcircuit is renamed to '`difpairw`' with a corresponding symbol as shown below.

```
*Differential NMOS pair with
*resistive load and differential output

*Noninverting input: Node 3
*Inverting input: Node 2
*Noninverting output: Node 4
*Inverting output: Node 5
*Supply voltage: Node 1
*Bias current: IB from node 6 to ground

.subckt difpairw 1 2 3 4 5 6

*Circuit description
R1 1 4 2.7k
R2 1 5 2.7k
M1 4 2 6 0 NMOS-BSIM L=0.7u W={W}
M2 5 3 6 0 NMOS-BSIM L=0.7u W={W}

.ends
```

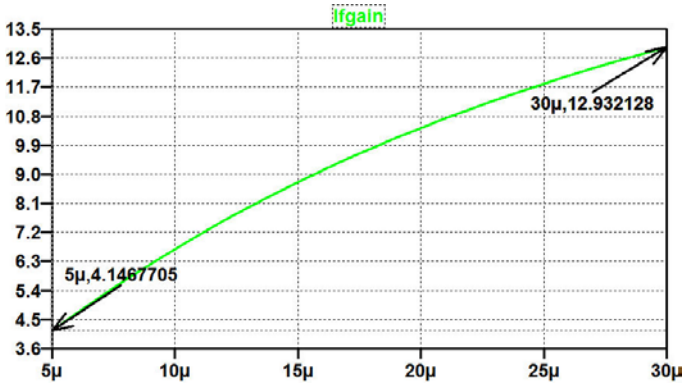


The testbench from problem 7.2 is modified by replacing the subcircuit '`difpair`' with '`difpairw`' and including a '.step' directive to sweep the channel width. Also, a '.measure' directive for finding the low-frequency gain is inserted as shown below. The resulting '.ac' simulation has many traces, see below.





In order to find the low-frequency gain versus channel width, we open the error log file and right click to 'Plot .step'ed .meas data'. The plot is shown below, and from the plot, we find a gain of 4.15 V/V for $W = 5$ µm and 12.9 V/V for $W = 30$ µm.



Appendix A – Errata

This appendix contains a list of known errors as of April 2016 in "CMOS Integrated Circuit Simulation with LTspice IV – a Tutorial Guide" (1st edition, 2015). Page references and line/figure references in the following tables are to this book.

Page	Line/figure	Correction
70	15	Original text: ..active region. Corrected text: .. active region. The active region is also called the saturation region, and the minimum value of V_{DS} for which the transistor is in the saturation region is called $V_{DS\text{sat}}$.

75	Figure 3.8	Both .model specifications contain the model parameters:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		For the NMOS transistor, the model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`
		For the PMOS transistor, the model parameters should be corrected to:
		`CGSO=0.21n CGBO=1p CGDO=0.21n`

76	Figure 3.9	In the SPICE Netlist, the model specifications are:
		`.model NMOS-SH nmos (Kp=190u Vto=0.57 Lambda=0.16 Gamma=0.50 Phi=0.7)`
		`+TOX=8n CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1m CJSW=0.4n)`
		`.model PMOS-SH pmos (Kp=55u Vto=-0.71 Lambda=0.16 Gamma=0.75 Phi=0.7)`
		`+TOX=8n CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1.5m CJSW=0.5n)`
		The model specifications should be corrected to:
		`.model NMOS-SH nmos (Kp=190u Vto=0.57 Lambda=0.16 Gamma=0.50 Phi=0.7`
		`+TOX=8n CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m CJSW=0.4n)`
		`.model PMOS-SH pmos (Kp=55u Vto=-0.71 Lambda=0.16 Gamma=0.75 Phi=0.7`
		`+TOX=8n CGSO=0.21n CGBO=1p CGDO=0.21n CJ=1.5m CJSW=0.5n)`

76	Figure 3.9	In the SPICE Error Log, the following three lines:
		`Cgsov: 2.00e-21 2.00e-21`
		`Cgdov: 2.00e-21 2.00e-21`
		`Cgbov: 2.00e-22 2.00e-22`
		should be corrected to:
		`Cgsov: 2.10e-15 2.80e-15`
		`Cgdov: 2.10e-15 2.80e-15`
		`Cgbov: 1.00e-18 1.00e-18`

Page	Line/figure	Correction
76	6-8	Original text: .. (The MOSIS Service 2014). Most foundries require non-disclosure agreements in order to provide detailed design information, but MOSIS does provide model files extracted from specific wafer lots, e.g. (The MOSIS Service: Wafer Electrical Test Data and SPICE Model Parameters 2014). Corrrected text: .. (The MOSIS Service 2014). However, most foundries require non-disclosure agreements in order to provide detailed design information.

87	Figure 3.21	In the .model specification, the model parameters are:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		The model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`

Page	Line/figure	Correction

88	Figure 3.22	In the SPICE Error Log, MOSFET Transistors, the following three lines:
		`Cgsov: 2.00e-21`
		`Cgdov: 2.00e-21`
		`Cgbov: 2.00e-22`
		should be corrected to:
		`Cgsov: 2.80e-15`
		`Cgdov: 2.80e-15`
		`Cgbov: 1.00e-18`

97	4-5	The following reference is now obsolete: The MOSIS Service: Wafer Electrical Test Data and SPICE Model Parameters 2014. Retrieved from https://www.mosis.com/pages/Technical/Testdata/tsmc-035-prm
102	7	Original text: .. $V_{to} = -0.557$ V; .. Corrected text: .. $V_{to} = -0.556$ V; ..
102	9	Original text: .. $V_{to} = 0.51$ V; .. Corrected text: .. $V_{to} = 0.520$ V; ..

105	Figure 4.2	In the .model specification, the model parameters are:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		The model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`

111	Figure 4.5	Both .model specifications contain the model parameters:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		For the NMOS transistor, the model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`
		For the PMOS transistor, the model parameters should be corrected to:
		`CGSO=0.21n CGBO=1p CGDO=0.21n`

111	Figure 4.6	Both .model specifications contain the model parameters:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		For the NMOS transistor, the model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`
		For the PMOS transistor, the model parameters should be corrected to:
		`CGSO=0.21n CGBO=1p CGDO=0.21n`

Page	Line/figure	Correction

112	Figure 4.7	In both SPICE Error Log files, the following three lines:
		`Cgsov: 4.00e-21 4.00e-21 3.80e-21`
		`Cgdov: 4.00e-21 4.00e-21 3.80e-21`
		`Cgbov: 2.00e-22 2.00e-22 2.00e-22`
		should be corrected to:
		`Cgsov: 4.20e-15 4.20e-15 5.32e-15`
		`Cgdov: 4.20e-15 4.20e-15 5.32e-15`
		`Cgbov: 1.00e-18 1.00e-18 1.00e-18`

115	12	Original text: .. compared to the current in M_3 in order .. Corrected text: .. compared to the current in M_2 in order ..

116	Figure 4.10	In the .model specification, the model parameters are:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		The model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`

117	Figure 4.11	In both SPICE Error Log files, the following three lines:
		`Cgsov: 2.00e-22 2.00e-21 3.40e-21`
		`Cgdov: 2.00e-22 2.00e-21 3.40e-21`
		`Cgbov: 2.00e-22 2.00e-22 2.00e-22`
		should be corrected to:
		`Cgsov: 2.80e-16 2.80e-15 4.76e-15`
		`Cgdov: 2.80e-16 2.80e-15 4.76e-15`
		`Cgbov: 1.00e-18 1.00e-18 1.00e-18`

120
123
	Figure 4.13
	Figure 4.17
		In the .model specification, the model parameters are:
		`CGSO=0.2f CGBO=0.2f CGDO=0.2f`
		The model parameters should be corrected to:
		`CGSO=0.28n CGBO=1p CGDO=0.28n`

126	13-14	v_{in} should be corrected to v_{id}
132	11-12	Original text: We can achieve this by defining a parameter M with a value of -1 for common mode gain, 0 for differential gain and $+1$ for power supply rejection. Corrected text: We can achieve this by defining a parameter M with a value of 1 for common mode gain, 2 for differential gain and 3 for power supply rejection.
142	16-17	Original text: .. to have a saturation voltage $\lvert V_{GS} - V_t \rvert$ of less than 50 mV, .. Corrected text: .. to have a saturation voltage $\lvert V_{DS\text{sat}} \rvert$ of less than 50 mV, ..

Page	Line/figure	Correction

143	Figure P4.4	In the model specification, the last two lines are:
		`+CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1m)`
		`+CJSW=0.4n)`
		They should be corrected to:
		`+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1m`
		`+CJSW=0.4n)`

144	Figure P4.5	In the model specification, the last two lines are:
		`+CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1.5m)`
		`+CJSW=0.4n)`
		They should be corrected to:
		`+CGSO=0.21n CGBO=1p CGDO=0.21n CJ=1.5m`
		`+CJSW=0.4n)`

145	Figure P4.8	In the PMOS model specification, the last two lines are:
		`+CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1.5m`
		`+CJSW=0.4n KF=5e-26)`
		They should be corrected to:
		`+CGSO=0.21n CGBO=1p CGDO=0.28n CJ=1m`
		`+CJSW=0.4n KF=5e-26)`
		In the NMOS model specification, the last two lines are:
		`+CGSO=0.2f CGBO=0.2f CGDO=0.2f CJ=1m`
		`+CJSW=0.4n KF=1e-25)`
		They should be corrected to:
		`+CGSO=0.28n CGBO=1p CGDO=0.28n CJ=1.5m`
		`+CJSW=0.4n KF=1e-25)`

146	4	Original text: 4.3: $W_1 = 30$ µm; $W_2 = 370$ µm; $W_3 = 3$ µm; $W_4 = 37$ µm; .. Corrected text: 4.3: $W_1 = 30$ µm; $W_2 = 240$ µm; $W_3 = 3$ µm; $W_4 = 24$ µm; ..
146	5	Original text: .. $r_o = 1019$ Ω; $I_{D1} = I_{D2} = 18.3$ µA; Corrected text: .. $r_o = 1005$ Ω; $I_{D1} = I_{D2} = 18.9$ µA;
146	8	Original text: 4.5: $V_{IN} = 692.40$ mV; $A_{voc} = 87$ dB, $r_o = 66$ MΩ, $r_m = 439$ kΩ. Corrected text: 4.5: $V_{IN} = 693.687$ mV; $A_{voc} = 84$ dB, $r_o = 48$ MΩ, $r_m = 430$ kΩ.

<table>
<tr><th>Page</th><th>Line/figure</th><th>Correction</th></tr>
<tr><td>146</td><td>12</td><td>Original text:
4.7: $V_{\text{off}} = -4.2$ mV; $GBW = 60$ MHz; CMRR = 66 dB; PSRR = 57 dB.
Corrected text:
4.7: $V_{\text{off}} = -4.2$ mV; $GBW = 60.7$ MHz; CMRR = 66.4 dB; PSRR = 56.6 dB.</td></tr>
<tr><td>187</td><td>Figure 6.6</td><td>Original text i figure caption:
.. and temperature W for an NMOS transistor ..
Corrected text:
.. and temperature for an NMOS transistor ..</td></tr>
<tr><td>210</td><td>6-9</td><td>Original text:
Process corners: (SN, SP, C_L) = (-1, -1, 1.7 pF): $GBW = 85.5$ MHz.
(SN, SP, C_L) = (1, -1, 1.7 pF): $GBW = 100.8$ MHz.
(SN, SP, C_L) = (-1, 1, 1.3 pF): $GBW = 112.3$ MHz.
(SN, SP, C_L) = (1, 1, 1.3 pF): $GBW = 133.2$ MHz.
Corrected text:
Process corners:
<table>
<tr><th>NMOS</th><th>PMOS</th><th>C_L</th><th>Unity-gain frequency</th></tr>
<tr><td>slow</td><td>slow</td><td>fast</td><td>111.3 MHz</td></tr>
<tr><td>fast</td><td>slow</td><td>fast</td><td>131.8 MHz</td></tr>
<tr><td>slow</td><td>fast</td><td>fast</td><td>112.3 MHz</td></tr>
<tr><td>fast</td><td>fast</td><td>fast</td><td>133.2 MHz</td></tr>
<tr><td>slow</td><td>slow</td><td>slow</td><td>85.5 MHz</td></tr>
<tr><td>fast</td><td>slow</td><td>slow</td><td>100.8 MHz</td></tr>
<tr><td>slow</td><td>fast</td><td>slow</td><td>86.3 MHz</td></tr>
<tr><td>fast</td><td>fast</td><td>slow</td><td>101.9 MHz</td></tr>
</table></td></tr>
<tr><td>210</td><td>10</td><td>Original text:
.. slow processes: $t_{delay} = 191$ ps.
Corrected text:
.. slow NMOS transistor, fast PMOS transistor: $t_{delay} = 199$ ps.</td></tr>
<tr><td>210</td><td>11</td><td>Original text:
6.5: Mean value of GBW: 85.6 MHz. Standard deviation: 3.6 MHz.
Corrected text:
6.5: Mean value of GBW: 85 MHz. Standard deviation: 4 MHz.</td></tr>
<tr><td>235</td><td></td><td>Voltage controlled current source:
Original text:
.. see page 29.
Corrected text:
.. see page 28.</td></tr>
</table>

Page	Line/figure	Correction
235		Voltage controlled voltage source: Original text: .. see page 29. Corrected text: .. see page 28.
245 - 247		**Index word** — **Original reference** — **Corrected reference** .meas, .measure — 60,189 — 59, 189 .noise — 17, 127, 135 — 17, 127, 136 Bode plot — 64 — 48 Noise — 135 — 136 Process, voltage and temperature variations, PVT — 180 — 179 Simulation AC analysis — 16, 48, 239 — 17, 48, 239 DC op pnt — 16, 238 — 17, 238 DC sweep — 16, 22, 238 — 17, 22, 238 DC Transfer — 16, 32, 239 — 17, 32, 239 Noise — 16, 127, 135 — 17, 127, 135 Transient — 16, 44, 239 — 17, 44, 239